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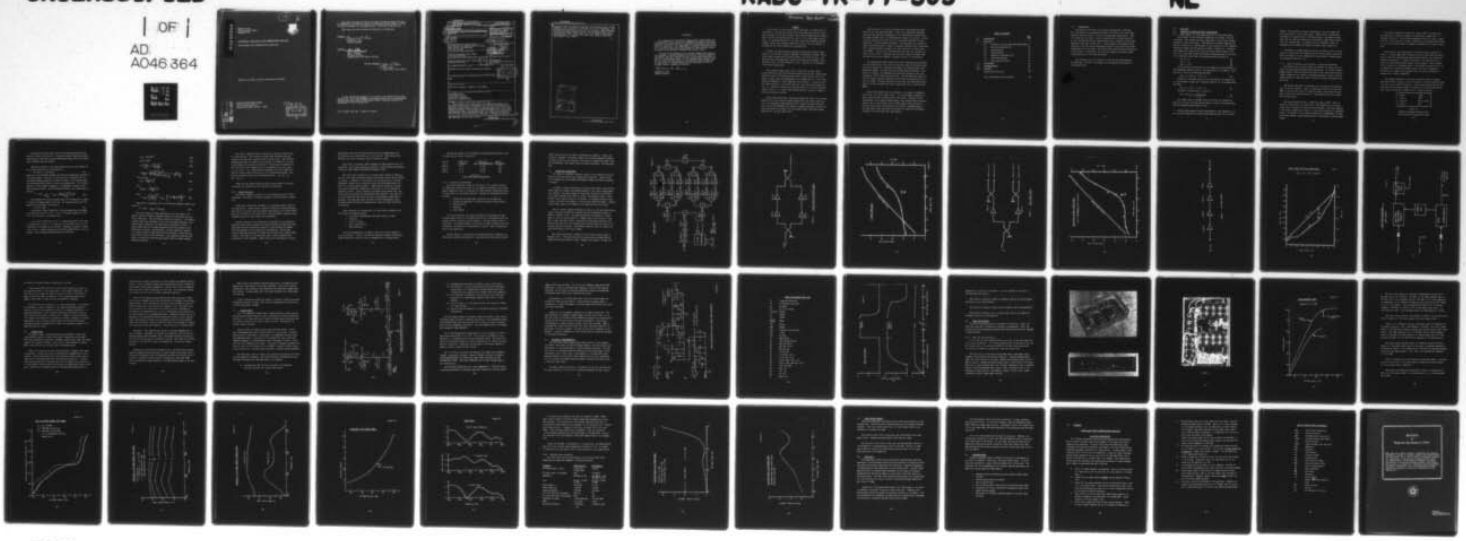

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RADC-TR-77-305
Final Technical Report
September 1977

EXPERIMENTAL LINEAR SOLID STATE COMMUNICATIONS AMPLIFIER

Ford Aerospace and Communications Corporation

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ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, New York 13441

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REPORT DOCUMENTATION PAGE

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1. REPORT NUMBER: RADC-TR-77-305	2. GOVT ACCESSION NO.
3. RECIPIENT'S CATALOG NUMBER	
4. TITLE (and Subtitle): EXPERIMENTAL LINEAR SOLID STATE COMMUNICATIONS AMPLIFIER.	5. TYPE OF REPORT & PERIOD COVERED: Final Technical Report. May 1976 — July 1977
	6. PERFORMING ORG. REPORT NUMBER: N/A
7. AUTHOR(s): J. Werry	8. CONTRACT OR GRANT NUMBER(s): F30602-76-C-0271
9. PERFORMING ORGANIZATION NAME AND ADDRESS: Ford Aerospace and Communications Corporation, WDL Division, 3939 Fabian Way, Palo Alto CA 94303	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: 62702F 55730391
11. CONTROLLING OFFICE NAME AND ADDRESS: Rome Air Development Center (DCCT), Griffiss AFB NY 13441	12. REPORT DATE: September 1977
	13. NUMBER OF PAGES: 48
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office): Rome Air Development Center (DCCT), Griffiss AFB NY 13441	15. SECURITY CLASS. (of this report): UNCLASSIFIED
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE: N/A

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

Same

18. SUPPLEMENTARY NOTES

RADC Project Engineer: Lawrence B. Sues (DCCT)

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Telecommunications
Linear Amplification
Field Effect Transistors
Microwave Integrated Circuit

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The objective of the linear solid state communications effort was to determine the feasibility of developing a five (5) watt linear solid state amplifier having a minimum efficiency of ten (10) percent, third order intermodulation products down by 30 dBc, and operating within the 7.1 to 8.4 GHz communications band. An experimental model of a linear solid state amplifier was developed, tested, and delivered under this contract for the purpose of determining the above feasibility and objectives. The amplifier which was →

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developed, tested, and delivered displayed 3 watts of power output, 160 MHz bandwidth at the -1 dB points, -30 dBc IMD, and 35 dB of linear gain. The saturated power output was 6.5 watts with 33 dB of gain. Linear efficiency was 5% and saturated efficiency was 10%. Group delay was better than 0.8 nanoseconds per 14 MHz. Noise figure was 8.7 dB. Phase vs power output was approximately 0.5 degree per dB in the linear regions of operation. Input VSWR was 1.25 or better.

Evaluation

The conversion of the Defense Communications System (DCS) from a predominently analog system to a predominently digital system has resulted in the use of efficient modulation techniques which require linear RF amplifiers. This requirement is currently being met by the use of traveling wave tubes (TWT) backed off from saturated output by several dB to minimize intermodulation product noise.

The amplifier developed on this contract demonstrates that recent advances in Gallium Arsenide Field Effect Transistor (GaAsFET) performance have made feasible the use of solid-state amplifiers in place of traveling-wave tubes in 8 GHz communications systems. GaAs FET amplifiers are considered to have potential applications both for new radios of improved design and for replacement of TWT in existing radios to improve reliability.

Lawrence B. Sues

LAWRENCE B. SUES
Project Engineer

SUMMARY

The objective of this project was to determine the feasibility of developing a five (5) watt linear solid state amplifier having a minimum efficiency of ten (10) percent, third order intermodulation products down by 30 dB, and operating within the 7.1 to 8.4 GHz communications band. An experimental model of a linear solid state amplifier was developed, tested, and delivered under this contract for the purpose of determining the above feasibility and objectives.

Briefly, the specification required an amplifier having a power output of one (1) watt minimum, 400 MHz 3 dB bandwidth minimum, -30 dB third order intermodulation products (IMD), with 30 dB of gain. The amplifier which was developed, tested, and delivered displayed 3 watts of power output, 160 MHz bandwidth at the -1 dB points, -30 dBc IMD, and 35 dB of linear gain.

The saturated power output was 6.5 watts with 33 dB of gain. Linear efficiency was 5% and saturated efficiency was 10%. Group delay was better than 0.8 nanoseconds per 14 MHz. Noise figure was 8.7 dB. Phase vs power output was approximately 0.5 degree per dB in the linear regions of operation. Input VSWR was 1.25 or better. No spurious outputs were observed in the output spectrum. The experimental model was built to commercial standards and was delivered in a suitable enclosure complete with a D. C. power conditoning/protection circuit in order to prevent accidental failures.

Fujitsu GaAs Field Effect Transistors (FET) were used in the entire design due to their superior power capabilities over other vendor devices. The parameters were measured with a network analyzer and matching circuits were designed and tested on Alumina substrates as were the power splitters and dividers for the parallel power combining process required for the high power output.

Many new types of technical problems were encountered when working with the high power GaAs FET's. Due to the GaAs FET's extremely high gain and unstable S-parameters at low frequencies, extensive low Q by-pass networks had to be developed for biasing the devices. Another technical problem that exists with the high power GaAs FET's is the difficulty of obtaining wide bandwidth. This problem can be solved by using chip devices without cases to eliminate unwanted input inductances and by using 90 degree hybrids in all input circuits to cancel high input VSWR's. Care must be exercised when applying bias voltages for turn-on and turn-off. Negative gate bias must always be present when positive drain bias is applied to prevent burn-out of the devices.

The experimental model Linear Solid State Communications Amplifier that was developed on this contract has proven that Field Effect Transistors are definitely a feasible replacement for Traveling Wave Tube Amplifiers (TWTA). The FET amplifier exceeds TWTA performance in the areas of linearity or Intermodulation Distortion Products, AM to PM conversion, noise figure and group delay. The FET amplifier power output for linear output and associated efficiency are competitive with that of a TWTA. Although unproven at this time, FET amplifiers should prove to be more reliable and have a higher mean time to failure than TWTA's.

Further development work is necessary in the areas of bandwidth, efficiency, and higher power output. It is also deemed reasonable to expect improved IMD performance with future work. Improved circuit optimization using computer aided design, more sophisticated mechanical design, use of chip devices, use of higher power output devices or more multiple stages, and elimination of directly cascaded stages in the high power output portions will provide the improved performance necessary for future amplifier requirements.

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1.0 INTRODUCTION

The technical task that this contract required was to develop, test, and deliver one experimental model of a linear solid state amplifier with specifications to suit data transmission requirements. Some R & D work had been done by various manufacturers of power GaAs FET's in test fixtures and single stage circuits, but a complete linear power amplifier chain had not been built. Ford Aerospace and Communications Corporation has been doing development work with high power Field Effect Transistors for 2-1/2 years. The solid state linear amplifier described in this report is believed to be the first complete and highest power X-Band amplifier in this new technology.

The following text will endeavor to describe what was designed, and developed, how well it performs, and the expected performance of future amplifiers.

2.0 MAIN TEXT

2.1 ANALYSIS OF LINEAR AMPLIFIER REQUIREMENTS

2.1.1 Requirements for Linear Amplification of a Two Tone Signal

When signals of two different frequencies are summed, they add vectorally. This causes the signal amplitude to vary as the voltages periodically add and subtract. This amplitude envelope completes one cyclical variation in a period equal to the reciprocal of the frequency difference between the two signals as shown in Figure 2.1. Assuming one voltage has a value of one, and the ratio second voltage to the first is k, the peak voltage and minimum voltage measured at the crest of an individual cycle over one difference period is given by:

$$Vp = 1 + k \tag{1}$$

$$Vm = 1 - k \tag{2}$$

$$Pav = 1 + k^2 \tag{3}$$

At the instant of time when the two signals are simultaneously at their maximum voltage and are at the same polarity, the power at that instant of time is the Peak Envelope Power.

$$PEP = (1 + k)^2 = 1 + k^2 + 2k \tag{4}$$

Similarily, the power output at the point where the signals are at their maximum voltage and of opposite polarity is the Minimum Envelope Power.

$$MEP = (1 - k)^2 = 1 + k^2 - 2k \tag{5}$$

The peak to average ratio is given by

$$P/A = PEP/_{Pav} = \frac{1 + k^2 + 2k}{1 + k^2} \tag{6}$$

The largest peak to average ratio occurs when the signals are equal (k = 1) and, the peak envelope power is twice the average power and the minimum envelope power is zero.

This envelope imposes certain requirements on the amplifier if it is to produce essentially distortionless amplification of a two-tone

signal. The amplifiers transfer characteristic must be linear and continuous down to a zero input level. There can be no dead zones, hysteresis or instabilities at low drive levels. The amplifier must also have the inherent capability of providing a power output equal to twice the average power. No predistortion or feedback scheme can compensate for an amplifier lacking the power output capability.

Obviously, the power amplifier can not be driven so far into saturation on peaks that the transfer function becomes highly non-linear. This non-linearity can be compensated to some extent by linearization as discussed in Seccion 2.1.4.

2.1.2 Class of Operation and Linearity - Efficiency Trade-Offs

The definition of class of operation defined for vacuum tubes is useful for characterizing solid state amplifiers. It should be remembered, however, that the definitions tend to lose their rigor since at higher frequencies the effects of feedthrough power, transit time and charge storage in junctions tends to distort the axis crossings of the RF cycles.

The Class C amplifier is unsuitable for low distortion amplification of two tone signals. Since the amplifier conducts for less than 180° of the RF cycle, there is a definite signal level where the gain goes to zero which causes distortion. This amplifier has the highest DC to RF efficiency.

The Class A amplifier has a conduction angle of 360°. That is, there is no distortion of the RF cycle. This amplifier can be quite linear and is suitable for multiple octave designs. The chief drawback to the Class A amplifier is that it is the least efficient at saturated output. In addition, its DC power consumption is independent of signal level which causes a rapid deterioration of efficiency at reduced power levels.

The Class B amplifier conducts for exactly 180^{o} of the RF cycle. This amplifier in theory is capable of amplifying a signal with no envelope distortion. Its efficiency approaches that of a Class C amplifier and it also reduces its power consumption as the signal level drops so that its efficiency does not degrade as rapidly as the Class A amplifier.

Many devices, when operating at low current levels, become nonlinear. A Class B amplifier's current will go to zero under two equal signal conditions and depending upon device linearity, can cause intermodulation distortion. To reduce this effect, the amplifier can be biased to draw some quiescent current at zero signal. This increases device linearity at low power levels. This class of operation, AB, is intermediate in efficiency between Class A and Class B operation. Obviously, the larger the quiescents bias, the more the amplifier appears like a Class A amplifier.

The maximum theoretical efficiency obtainable from the various amplifiers shown in Table 2.1 are of interest to show the relative capabilities of each class of operation. Since these efficiencies are for ideal devices and lossless passive components, they only show how well each class of operation utilizes the D. C. power available.

Class C	> 80%
Class B	78.5%
Class AB	50% to 78.5%
Class A	50%

Table 2.1
Theoretical Maximum Efficiency for
Various Classes of Amplifier Operation

It should be further noted that the efficiencies quoted do not take device gain into account. In general, Class A operation yields higher gain so that when low gain devices are used, much of the efficiency differentials are reduced.

The power envelope of two equal signals (which is the square of the voltage envelope) can be described as

$$P = Pav\ (1 - \cos\ \Delta wt) \tag{7}$$

where w is the difference between the two equal frequencies and PAV is the average power. Note that if the function is averaged over the difference frequency period, the power is equal to the average power and the maximum power (PEP) is twice the average power. In a Class A amplifier, the DC power consumption is independent of power output below saturated output. The following efficiency relationship may be written

$$\eta = \eta\ SAT\ \frac{P}{P_{SAT}} = \eta_{SAT}\ \frac{P_{AV}\ (1 - \cos \Delta\ wc)}{2\ P_{AV}} \tag{8}$$

This assumes that the saturated output of the amplifier is equal to twice the average power or the PEP. By integrating (8) over the period of the envelope, the result is

$$\eta = 1/2\ \eta\ SAT \tag{9}$$

This means a Class A amplifier linearily amplifying a two equal tone signal will have its D. C. to R. F. efficiency reduced to one-half its efficiency at saturated output.

In a Class B amplifier, the R. F. current delivered to the load is proportional to the D. C. current and the RF power output is proportional to the square of the current. Assuming a constant voltage bias, the D. C. power consumption is directly proportional to the D.C. current. The following relationships can be written:

$$P_{out} = (k_1 Idc)^2 \tag{10}$$

$$P_{dc} = k_2 Idc \tag{11}$$

$$\eta = \frac{P_{out}}{P_{dc}} = \frac{(k_1 Idc)^2}{k_2 Idc} \tag{12}$$

$$\frac{\eta}{\eta_{SAT}} = \frac{(k_1 Idc)^2 / k_2 Idc}{(k_1 Idc_{SAT})^2 / k_2 Idc_{SAT}} = \frac{I_{dc}}{Idc_{SAT}} \tag{13}$$

and using 10

$$Idc = \frac{(P_{out})^{1/2}}{k_1} \tag{14}$$

and

$$Idc_{SAT} = \frac{(P_{SAT})^{1/2}}{k_1} \tag{15}$$

then

$$\eta = \eta_{SAT} \left(\frac{P_{out}}{P_{SAT}}\right)^{1/2} = \eta_{SAT} \left(\frac{1 - \cos \Delta wt}{2}\right)^{1/2} \tag{16}$$

When (16) is integrated over the difference frequency period, the result is

$$\eta = \frac{2}{\pi} \eta_{SAT} = 0.64 \eta_{SAT} \tag{17}$$

The result shows that when amplifying a two-tone signal, the Class B amplifier suffers a smaller reduction of efficiency than the Class A amplifier. This difference yields real benefits. For example, a Class A amplifier handling a 1-watt two-tone signal requires a saturated output capability of 2 watts with an efficiency of 20 %. A Class B amplifier for the same application need only achieve 15.6% efficiency at 2 watts. Alternatively, a Class B amplifier capable of 3.3 watts output at 20% efficiency will provide a 1-watt two-tone output with a 10% DC to RF efficiency. This operating condition provides a 2 dB back-off from saturated power output on peaks, greatly enhancing linearity.

Any class of amplifier may be operated in push-pull using a pair of active devices. This doubles the peak power available from the amplifier the same way a parallel pair of devices does. The push-pull configuration does not improve the linearity of an amplifier in terms of odd ordered cross product generation. The push-pull configuration will only cancel even ordered distortion products such as $2f_1$, $2f_2$, $f_1 + f_2$, and $f_1 - f_2$. These products generally fall well outside the band of interest and are filtered out by the matching networks. The distortion products which are troublesome are $2f_1 - f_2$, $2f_2 - f_1$, $3f_1 - 2f_1$, etc.

These are odd ordered products caused by odd ordered non-linearities which are unaffected by the push-pull configuration.

2.1.3 Device Selection

The types of devices available for this application are in three categories: bulk effect, bi-polar transistor, and field effect transistor.

Bulk effect devices are available in the required power range for this application. These devices, however, suffer from several drawbacks. They tend to be Class A devices drawing large amounts of no signal power. They have a tendency to be stable over a limited dynamic range and their transfer function is less linear than transistors.

Bipolar transistors are presently not available for the required frequency-power range although device manufacturers are developing them. High power bipolar transistors available to date (S-Band and C-Band) have been packaged in the common base configuration. The package inserts some lead inductance in series with the base which causes regeneration. The result is the amplifiers tend to have hysteresis and thresholds in their response. Newer devices are being made for linear

applications and have ballasted emitters which are degenerative and help equalize the current densities in the device. These devices are designed for Class A operation and are limited to 3 GHz.

Field Effect Transistors (FET) designed for power applications are available. Device power outputs in excess of 1 watt have been obtained at 8 GHz with power added efficiencies in excess of 25%.

The field effect transistor is a linear device capable of maintaining the third order distortion products 30 dB down without special design or biasing. In addition, efficiencies for FET are quoted at 1 dB gain compression rather than at saturated output providing some margin for back off to achieve good linearity. Under Class A operation, the gate is reversed biased with respected to the source to set the quiescent operating current. Class B operation increases this reverse bias, the circuit gain is reduced and increased RF drive required. The condition of high reverse and high drive can lead to gate-channel break-down on RF peaks. The resulting rapid increase in drive requirements causes the power added efficiency to decrease even though the drain efficiency has improved.

After reviewing the alternatives, the field effect transistor has been chosen for several reasons.

- o Can achieve required gain and power output at 8 GHz
- o Linearity
- o Ease of biasing
- o Device availability
- o High efficiency

The only disadvantage of the FET is that full Class B operation is not achievable. Even so, the FET can achieve in excess of 20% power added efficiency in Class A, which is adequate for this application.

The devices chosen for this design are manufactured by Fujitsu, Ltd. of Japan and are listed in Table 2-2.

Device	8 GHz Power Output	8 GHz Gain (at 1 dB Compression)	Drain Efficiency
FLC-08	0.6 W	6.0 dB	50%
FLC-15	1.0 W	5.0 dB	42%
FLC-30	1.9 W	4.0 dB	40%

Table 2-2
8 GHz FIELD EFFECT TRANSISTORS

2.1.4 Linearization Techniques

Distortion generally occurs at both ends of the transfer function. All amplifiers become non-linear as they approach saturated output while Class B amplifiers tend to loose gain at small signals causing distortion at that portion of the signal envelope. Methods for reducing distortion include:

- o Increasing the peak power capability of the amplifier
- o Biasing the amplifier to Class AB operation (from Class B)
- o Pre-distortion
- o Feedback
- o Feed forward

Biasing an amplifier for Class AB operation and keeping the peak envelope power below the 1 dB compression point of the amplifier are the easiest methods of assuring good linearity. The price paid is loss of efficiency. If adequate margin is available in terms of power output and efficiency, this method of linearization is viable. This technique was used on this amplifier.

Another source of non-linearity is phase distortion; therefore, an additional technique was employed in this amplifier design which signifi-

cantly improved the third order intermodulation products. During the tuning or alignment of parallel stages that utilized quadrature hybrids for power splitting and combining, the amplifier stages were phase tuned for minimum IMD. This method cancelled phase distortion, thus improving IMD.

2.2 FUNCTIONAL DESCRIPTION

The reader is referred to Figure 1 which is the complete block diagram of the Linear Solid State Communication Amplifier. Module level block diagrams and their module performance curves are shown in Figures 2 through 7.

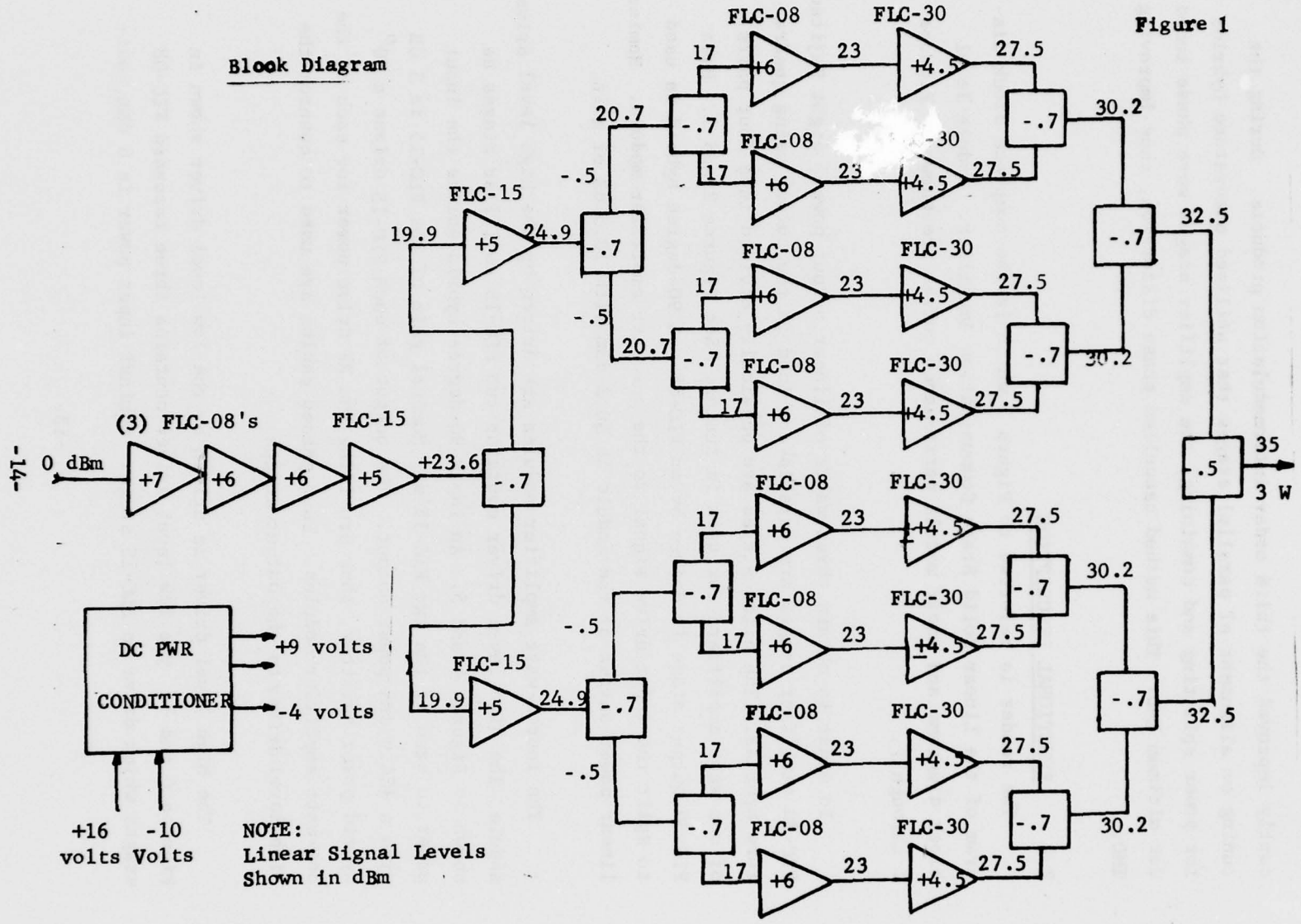
In order to obtain three watts of linear output power, eight Fujitsu FLC-30 amplifier stages are parallel combined in the output using quadrature hybrids. The eight stages are physically divided into four pairs of one watt amplifiers for ease in tuning. See Figures 2 and 3. Each FLC-30 output stage is driven by an FLC-08. A 90-degree hybrid is used to split the input drive signal to the one watt amplifier module. Nominal linear power output of the module is 30.2 dBm with 10.5 dB of gain.

The four 1-watt amplifier modules are driven by the high level driver module. The high level driver contains two FLC-15 amplifier stages as shown in Figures 4 and 5. An input 90-degree hybrid splits the input power to each of the two FLC-15's. Nominal gain of the FLC-15 is 5 dB with a +24.9 dBm power output. The output of each FLC-15 drives a 90^{o} hybrid power splitter, thus providing the RF drive power for each of the one-watt amplifier modules. Four phased cables are used to connect the high level driver to the output stages.

The high level driver is driven by the low level driver shown in Figures 6 and 7. The low level driver contains three cascaded FLC-08 stages which drive an FLC-15 stage. Nominal input power is 0 dBm, out-

Figure 1

Block Diagram



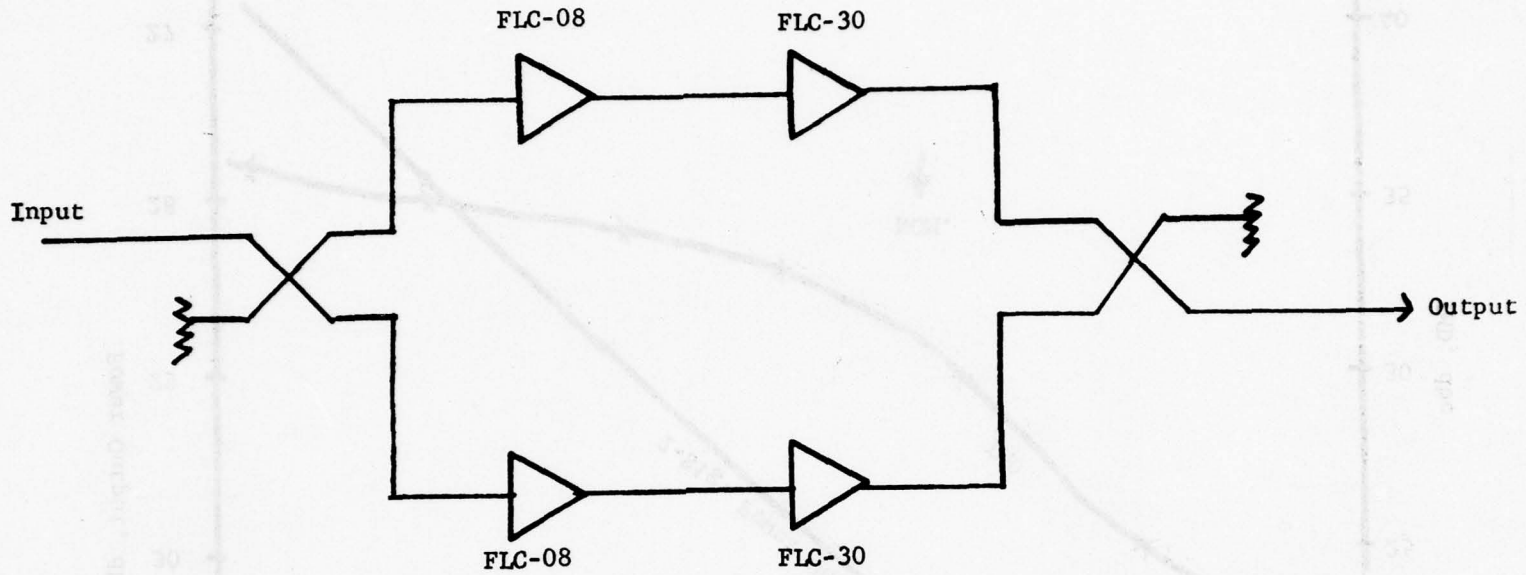


Figure 2 1-WATT LINEAR AMPLIFIER MODULE

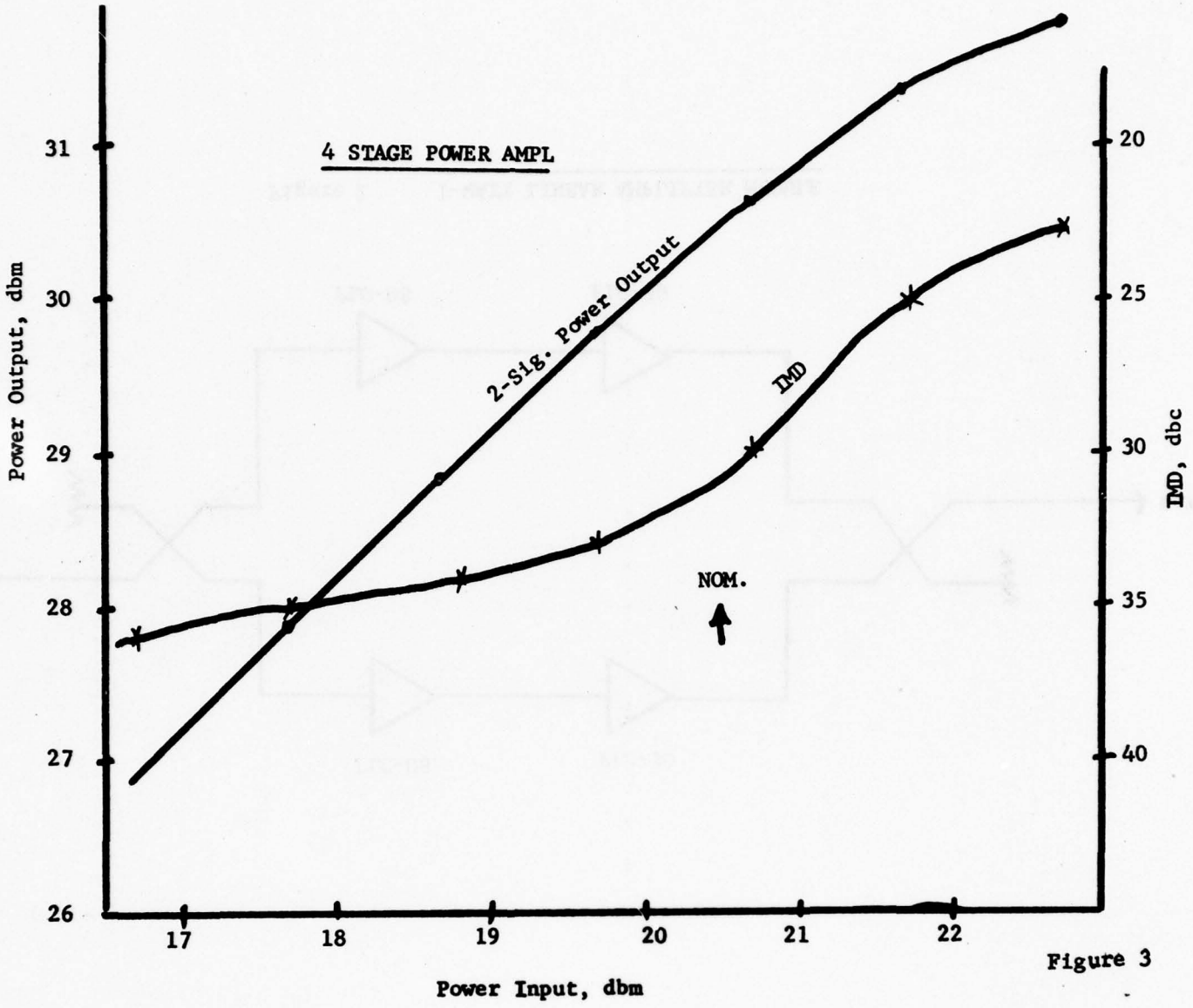

4 STAGE POWER AMPL
2-Sig. Power Output
IMD
NOM.
Power Output, dbm
IMD, dbc
Power Input, dbm
31
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Figure 3

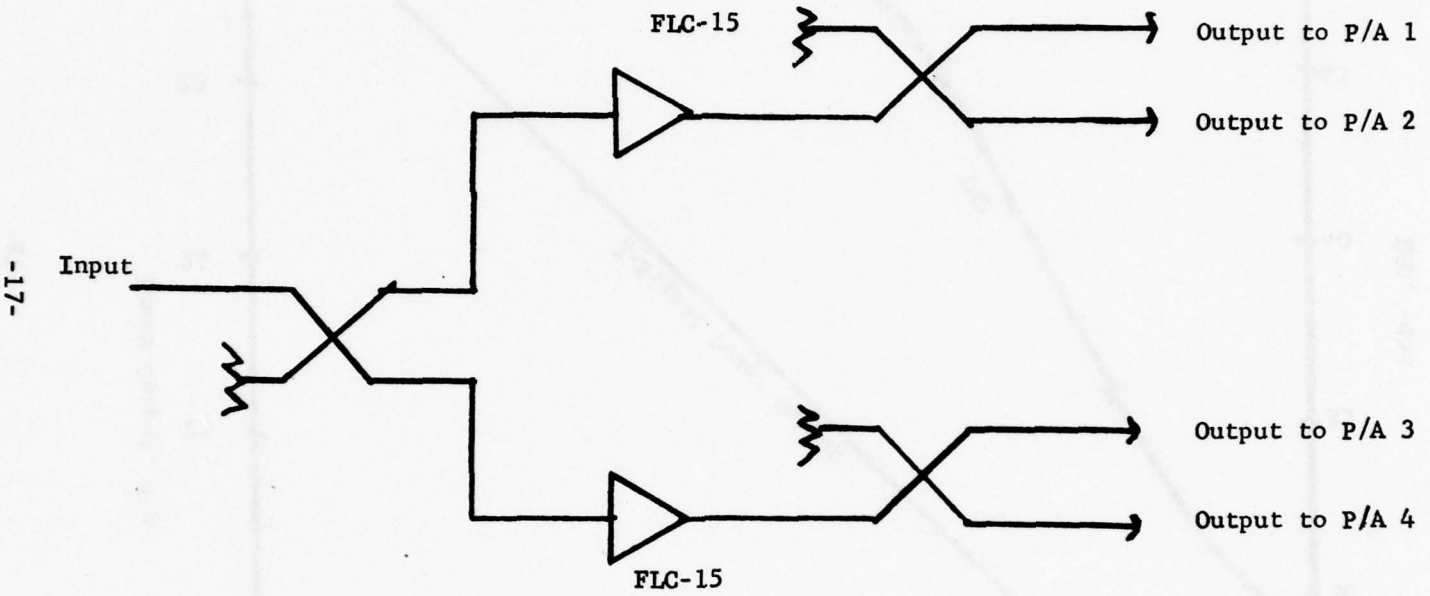
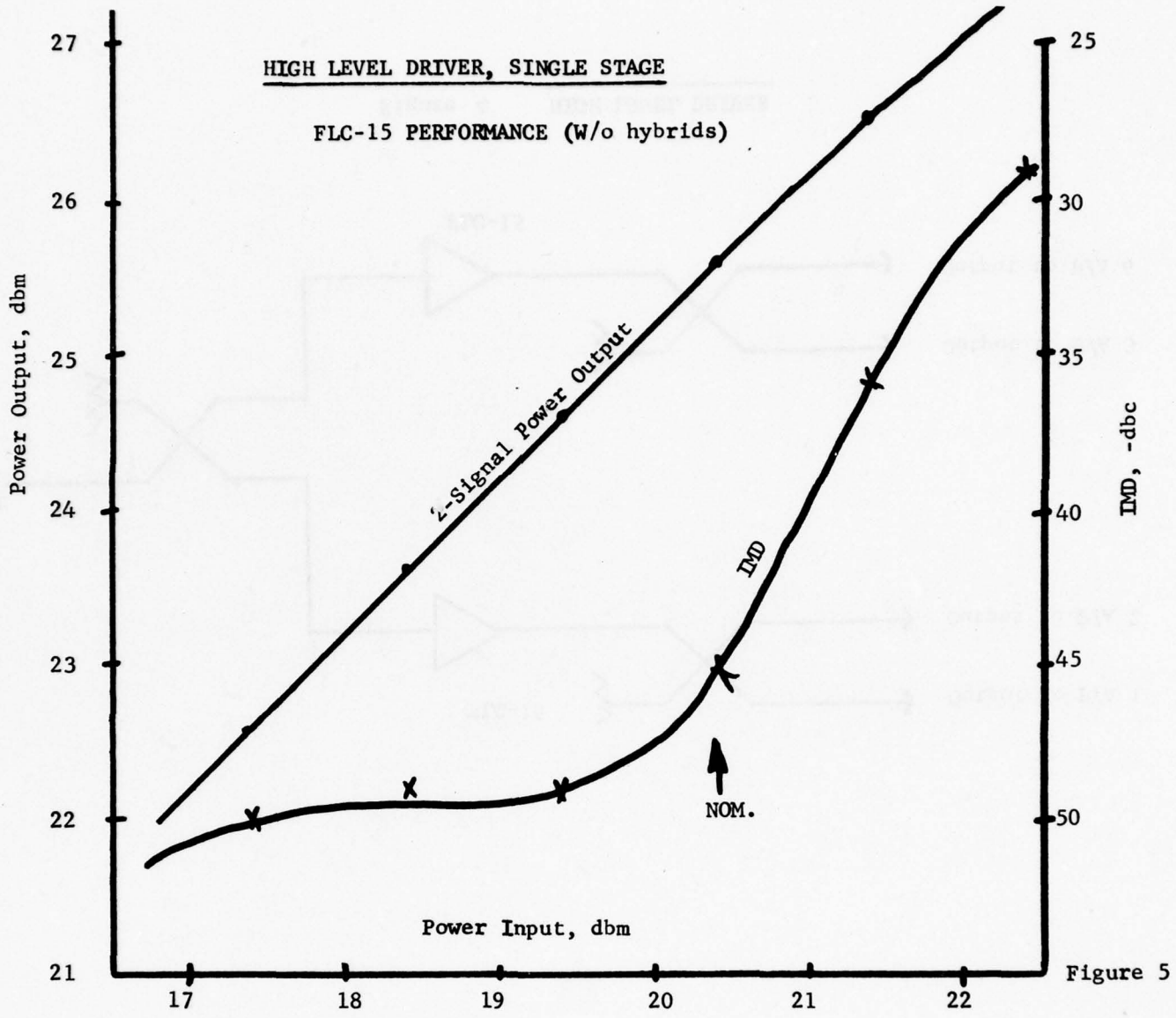


Figure 4 HIGH LEVEL DRIVER


HIGH LEVEL DRIVER, SINGLE STAGE
FLC-15 PERFORMANCE (W/o hybrids)
Power Output, dbm
IMD, -dbc
Power Input, dbm
2-Signal Power Output
IMD
NOM.
27
26
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22
21
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Figure 5

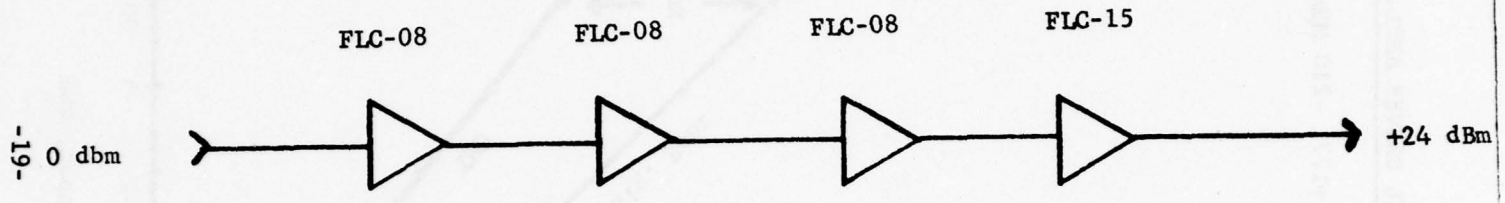
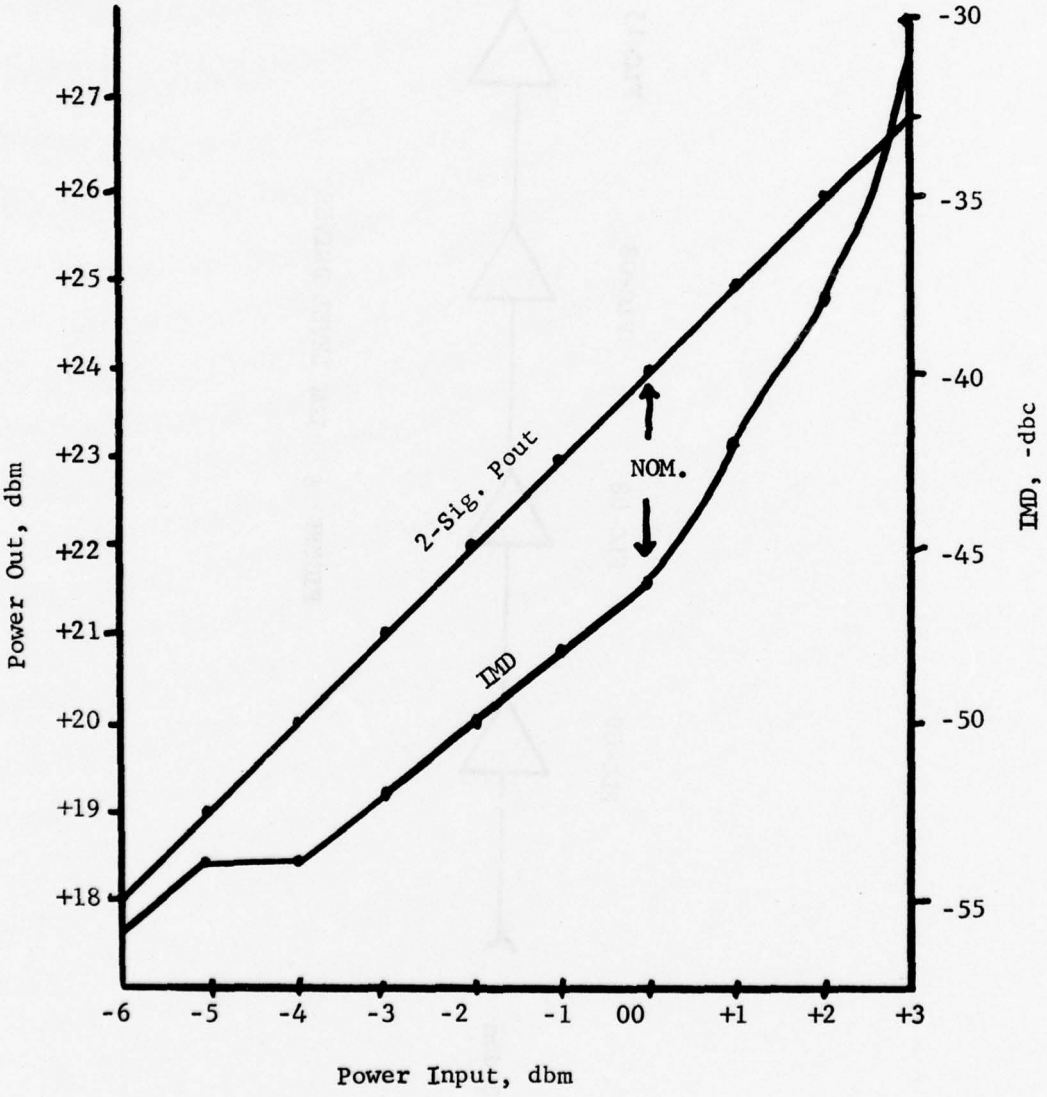


FIGURE 6 LOW LEVEL DRIVER

RADC 4-STAGE LOW LEVEL DRIVER AMPL. Fig. 7

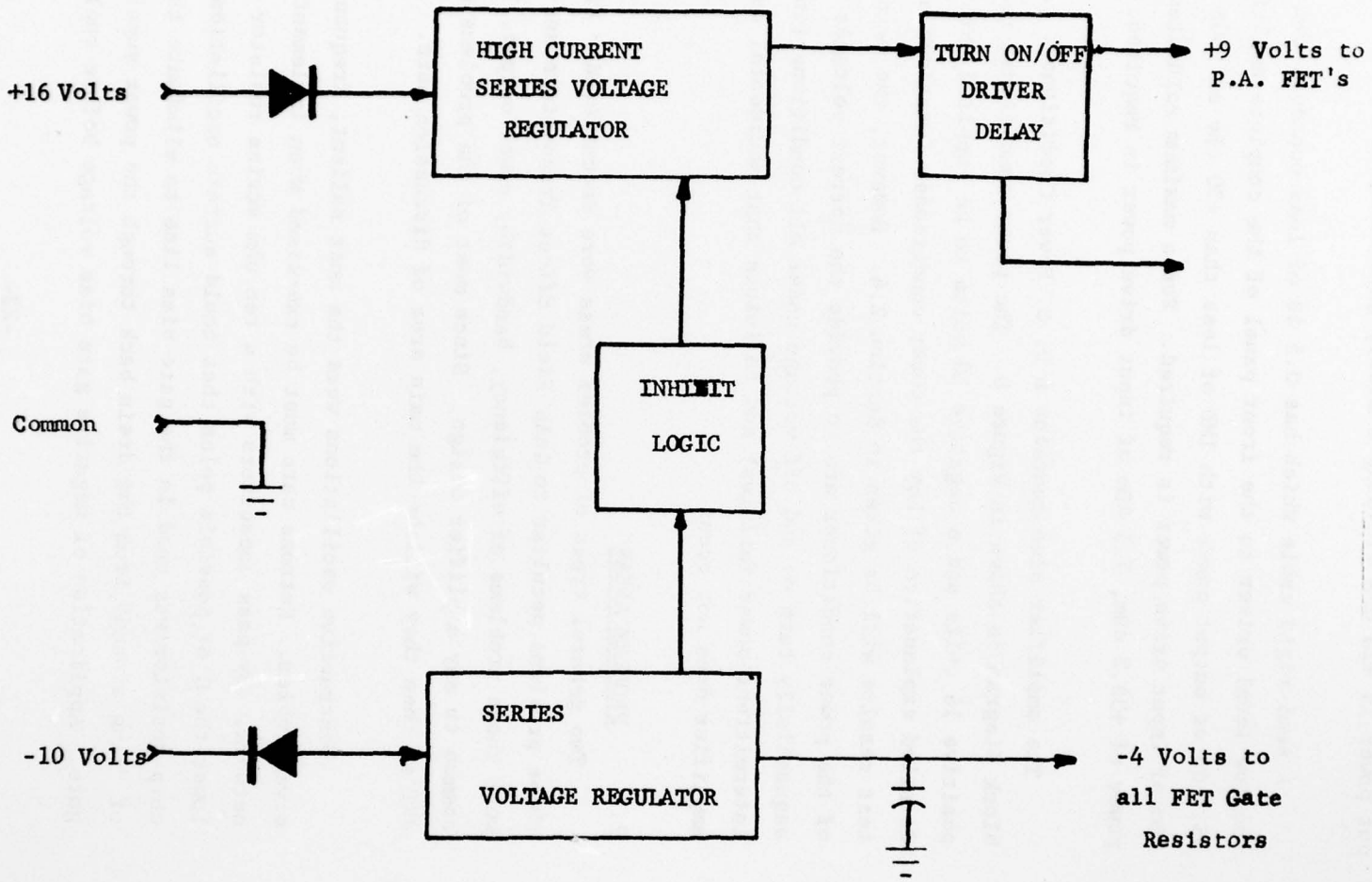
Bw $\pm$ 1 db = +177, -210 MHz



RADC POWER CONDITIONER

BLOCK DIAGRAM

Figure 8



put power is +24 dBm yielding a module gain of 24 dB.

A semi-rigid cable which has 0.5 dB of loss connects the input of the low level driver to the front panel of the complete amplifier. For 35.2 dB of output power with IMD of less than -30 dBc at 7500 MHz, 0.5 dBm of input drive power is required. For a maximum saturated output power of +38.2 dBm, 5.5 dBm of input drive power is required.

The amplifier also contains a D. C. Power Conditioner. A functional block diagram is shown in Figure 8. The power conditioner requires a positive 16 volts and a negative 10 volts to be supplied externally. A detailed explanation of how the power conditioner functions along with test results will be given in Section 2.4. However, the main functions of the power conditioner are to provide the correct voltages to the FET's, sequentially turn on and off voltage under all conditions (including intermittent power failures) and to insure that accidental damage to the amplifier does not occur.

2.3 PROBLEM AREAS

Two general types of problem areas were encountered. First were those problems peculiar to GaAs Field Effect Transistors and secondly, were those problems of efficiency, bandwidth, power output, IMD, and others common to any amplifier design. Since most of the problems do concern FET's, then they will be the main area of discussion here.

Destructive oscillations were the most salient, frequent, and expensive problem. Extreme care must be exercised when implementing the bias network. By-pass capacitors with a ten ohm series resistor were used to lower the Q of possible poles that could sustain oscillation. A series chip resistor was used in the gate bias line to eliminate the possibility of "ring around" from the drain back through the power supply leads to the gate. Application of negative gate bias voltage before application of

positive drain voltage is required to limit current and surpress oscillations. A brief laboratory power failure caused destruction of seven devices during initial final integration. This was due to loss of negative gate bias and no power conditioner at that time. All subsequent tuning and testing was done with the power conditioner employed.

Some of the original Fujitsu devices were light sensitive. Therefore, Fujitsu changed the cap over the devices to eliminate this problem. Unfortunately, this introduced an oscillation that occurred at very low drain voltages only. This oscillation appears to be a bulk effect type of oscillation, but has not been fully proven as such. Although the oscillation is non-destructive, it is at a sufficiently high power level to cause destruction of cascaded amplifiers. Sequential drain turn-on is employed in this amplifier's power conditioner circuit to solve the problem. The FLC-30's and FLC-15's are turned on first with the FLC-08's turned off as buffers. Then the FLC-08's, which do not appear to display this oscillation, are then turned on. Turn-off occurs in reverse order.

The gates of the GaAs FET are subject to voltage breakdown due to static charges. Personnel, hot plates, and soldering irons must all be grounded during module assembly until a discharge resistor is wired into the circuit from the gate bias network to ground. The value of the resistor used is 2 K ohms and is also an integral part of the bias voltage divider.

Bandwidth limitations were primarily due to the FET device package. Because packaged devices were used, the input (gate) path lengths and its associated inductance limits the bandwidth over which the device can be matched to microwave circuits without introducing a high input VSWR. Direct cascading of stages requires a low VSWR between stages to maintain low IMD.

Power output and likewise efficiency were about 1 dB lower than necessary due to high losses in the power combiners. This loss is mostly transmission line loss due to the relatively long distances between adjacent modules. Future designs will focus more attention upon eliminating this problem.

Another efficiency problem was caused by intensive tuning and optimum biasing for reduction of IMD. This could be compensated on future units by using lower drain voltages.

2.4 DESIGN DETAILS

All of the amplifier stages used a common substrate, bypass network, and mechanical chassis design in order to maintain low costs and maintain flexibility. All input and output stages utilized Alumina substrates one inch wide by one-half inch long by .025 inch thick. Metalization is chrome, copper, and gold.

Figure 9 shows the common single stage amplifier design. Eighth wave transformers were used to match directly to the device. An eighth wave section of line which is terminated in an impedance having an absolute magnitude equal to the device to be matched will have a real (not complex) impedance. A single quarter wave transformer is used to transform this real impedance to 50 ohms. A reasonable frequency response with low line loss can be obtained with this scheme. Because of device variations, Indium foil tuning was always necessary to achieve proper operation.

Low inductance, high Q, ceramic chip capacitors are used as DC blocks and low frequency by-passing. The basic RF circuit implementation bias technique developed for 8 GHz amplifiers is as follows:

a) A quarter-wave 100 ohm line is routed to the matching circuitry one-half wave length from the FET.

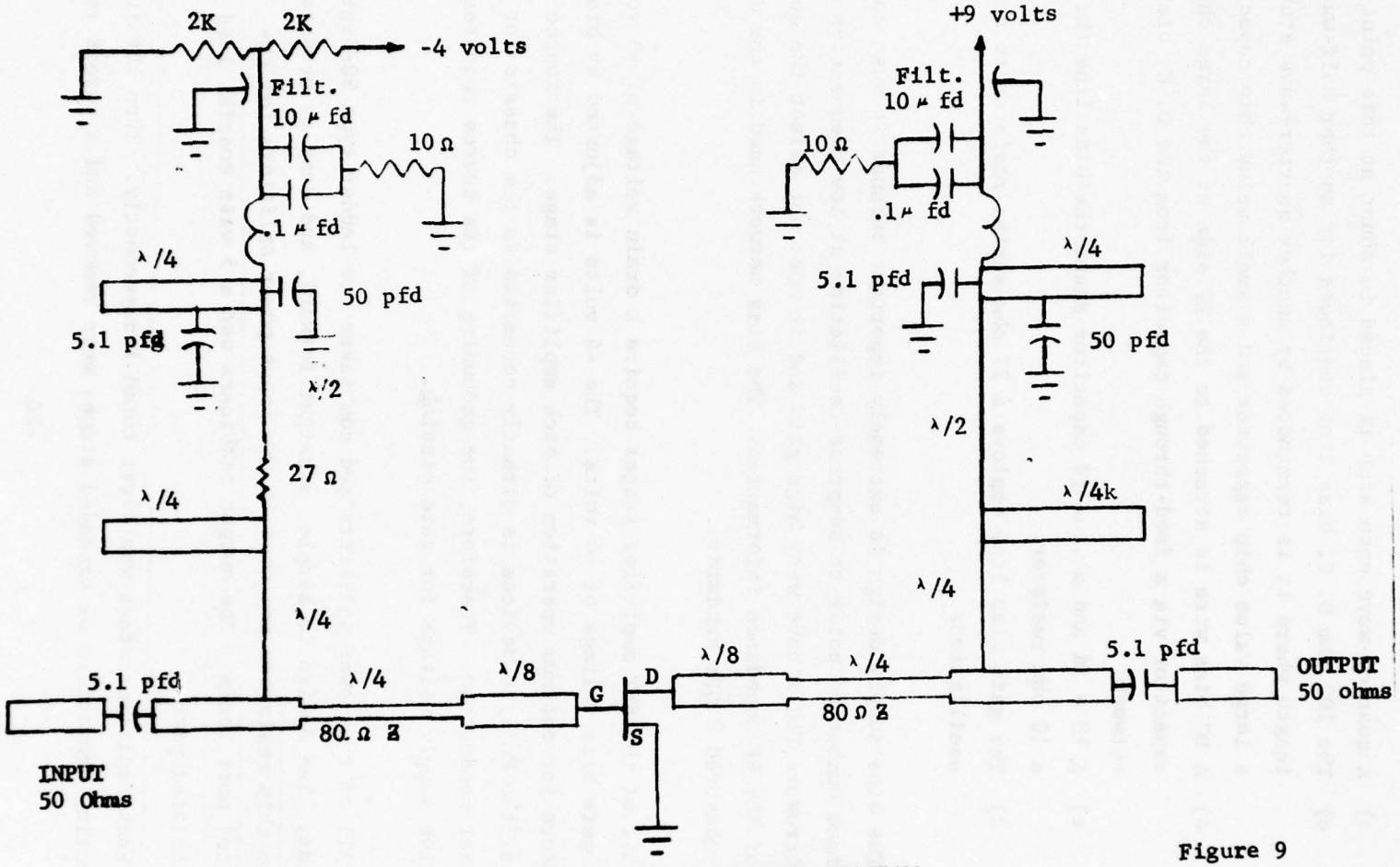


Figure 9

SINGLE STAGE FET AMPLIFIER CIRCUIT DIAGRAM

b) A quarter-wave open stub is placed in shunt at this point.

c) The 100 ohm D. C. bias line continues for another half-wave length where it is terminated by another quarter-wave stub, a large value chip capacitor and a small value chip capacitor.

d) A DC bias wire is attached to the RF side of the large chip capacitor via a feed-through capacitor from the D. C. bias network.

e) A 10 μ fd and a .1 μ fd capacitor shunt the bias line through a 10 ohm resistor.

f) The gate bias line employs a 27 ohm series resistor to surpress oscillations.

The bias supply design is extremely important because it must contain a minimum number of poles to suppress oscillation at low frequencies where the microwave FET's have very high gain and it must not affect the qualities of the RF impedance information. The bias network used in the design has a measured 2 GHz bandwidth.

All of the FET amplifier stages require a drain voltage of +9 volts and a gate bias voltage of -4 volts. The -4 volts is adjusted by bias resistors for optimum operation of each amplifier stage. The source contact of the Fujitsu devices is directly connected to the chassis for maximum heat conduction. Therefore, the grounding of the source requires a negative supply voltage for gate biasing.

All of the power splitters and combiners are ladder type 90-degree hybrids. The design is simple, straight forward, and easy to produce. 50-ohm chip resistors are used in the input power splitters for the isolated port loads. The output combiners use a 5 watt coaxial load at the isolated port.

Each amplifier stage was first tuned independently. Then the interconnecting connectors of cascaded stages were removed and a stress relief

jumper ribbon was installed. All of the two cascaded stages were tuned. Connectors on outputs and inputs were removed, a splitter and combiner installed, and the pairs of parallel stages were tuned for minimum IMD and maximum power output for a fixed RF input level.

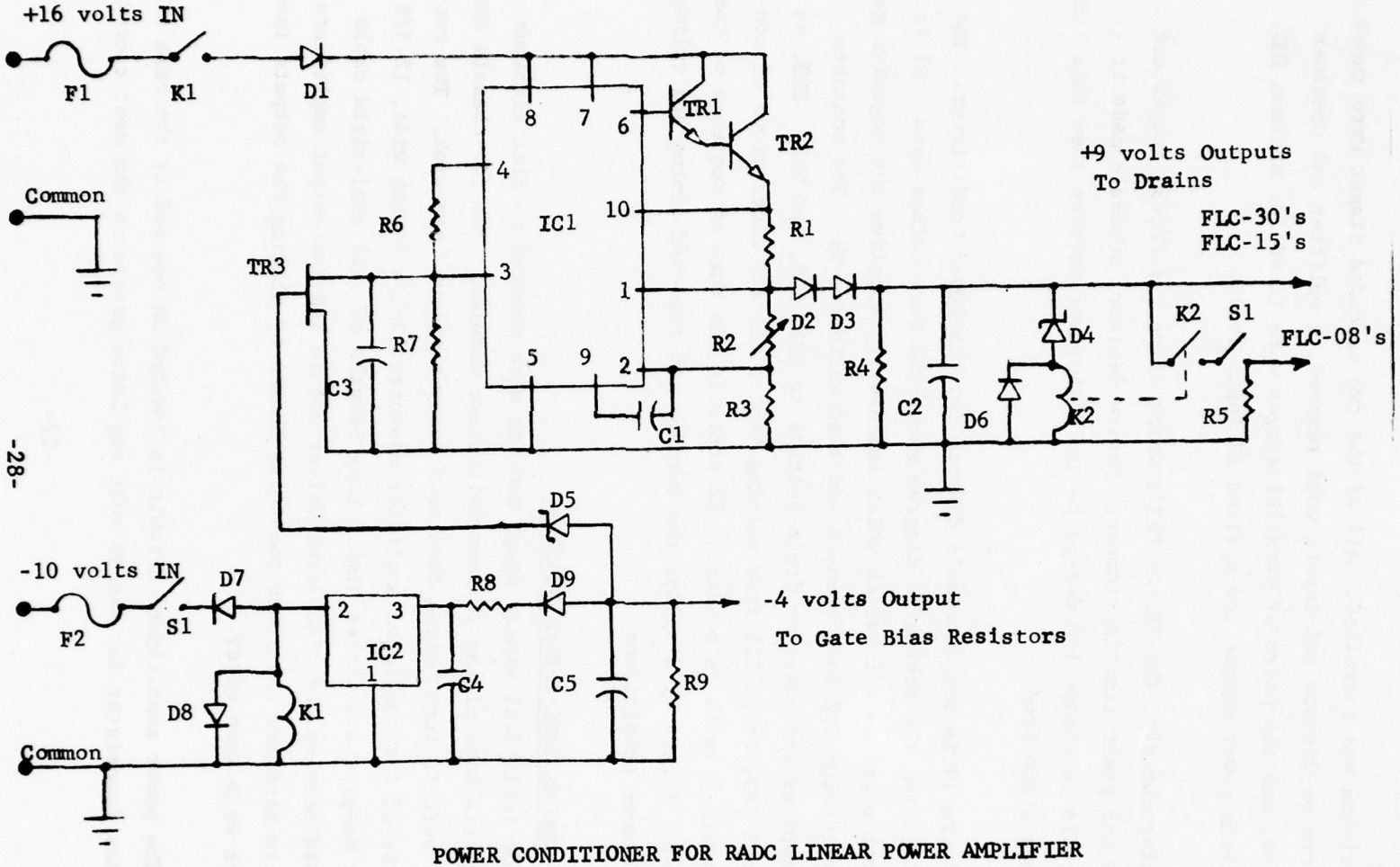
Unfortunately, the FLC-08 FET's which drive the FLC-30 stages are the IMD and power limiting factor. Device delivery schedule made it undesirable to change the design to use high power devices when this limitation was discovered.

Figure 10 is the schematic diagram for the Power Conditioner. The page following the schematic diagram shows the part values used. S1 is the front panel on-off switch which immediately supplies the negative gate voltage through IC2 upon turn-on and also activates K1. The contacts of K1 applies the positive drain voltage to IC1, TR1, and TR2. TR3, an N Channel FET, holds IC1 from turning "on" until the zener diode D5 conducts when -4 volts is present. K2 controls the turn on sequence of the FLC-08's. Figure 11 displays the turn-on and turn-off timing and voltages of the power conditioner.

2.5 MECHANICAL IMPLEMENTATION

The individual single stage modules were mounted on flat aluminum sub-chassis base plates to form multistage modules. The sub-chassis base plates were in turn bolted down to a heavy aluminum heat-sink. The overall size of the completed amplifier measures 17-1/4 inches wide, 12-5/8 inches deep, and 4 inches high. Long lengths of .141 semi-rigid cable were used between the high level driver module and the output amplifiers so as to minimize the power combining losses by placing the outputs face to face with each other.

The power conditioner circuit is located on one end of the heat sink. The pass transistor for the +9 volt regulator generates the most concen-



POWER CONDITIONER FOR RADC LINEAR POWER AMPLIFIER

Figure 10

POWER CONDITIONER PARTS LIST

F1	8 Amp Fast-Blow Fuse
F2	1/2 Amp Fast-Blow Fuse
K1	PB GA17D
K2	PB, 6 volt Relay
D1,D2,D3	1N1190
D4	1N750A
D5	1N746A
D6,D7, D8,D9	1N649
TR1	2N5337
TR2	2N5632
TR3	N Channel Junction FET
IC1	μA723
IC2	Lm 120H
S1	DPST Switch
R1	.067 ohm Wire-wound
R2	500 ohm 2W Pot
R3	680 ohm, 1/4 W
R4	120 ohm, 2W
R5	75 ohm, 2W
R6	1.6 K ohm, 1/4 W
R7	7.5 K ohm, 1/4 W
R8	S.A.T., Nom. 10 Ω, 2 W
R9	S.A.T., Nom. 300 ohm, 1/4 W
C1	.001 μ fd, CK05
C2	500 μ fd
C3	3.3 μ fd
C4	50 μ fd
C5	1000 μ fd

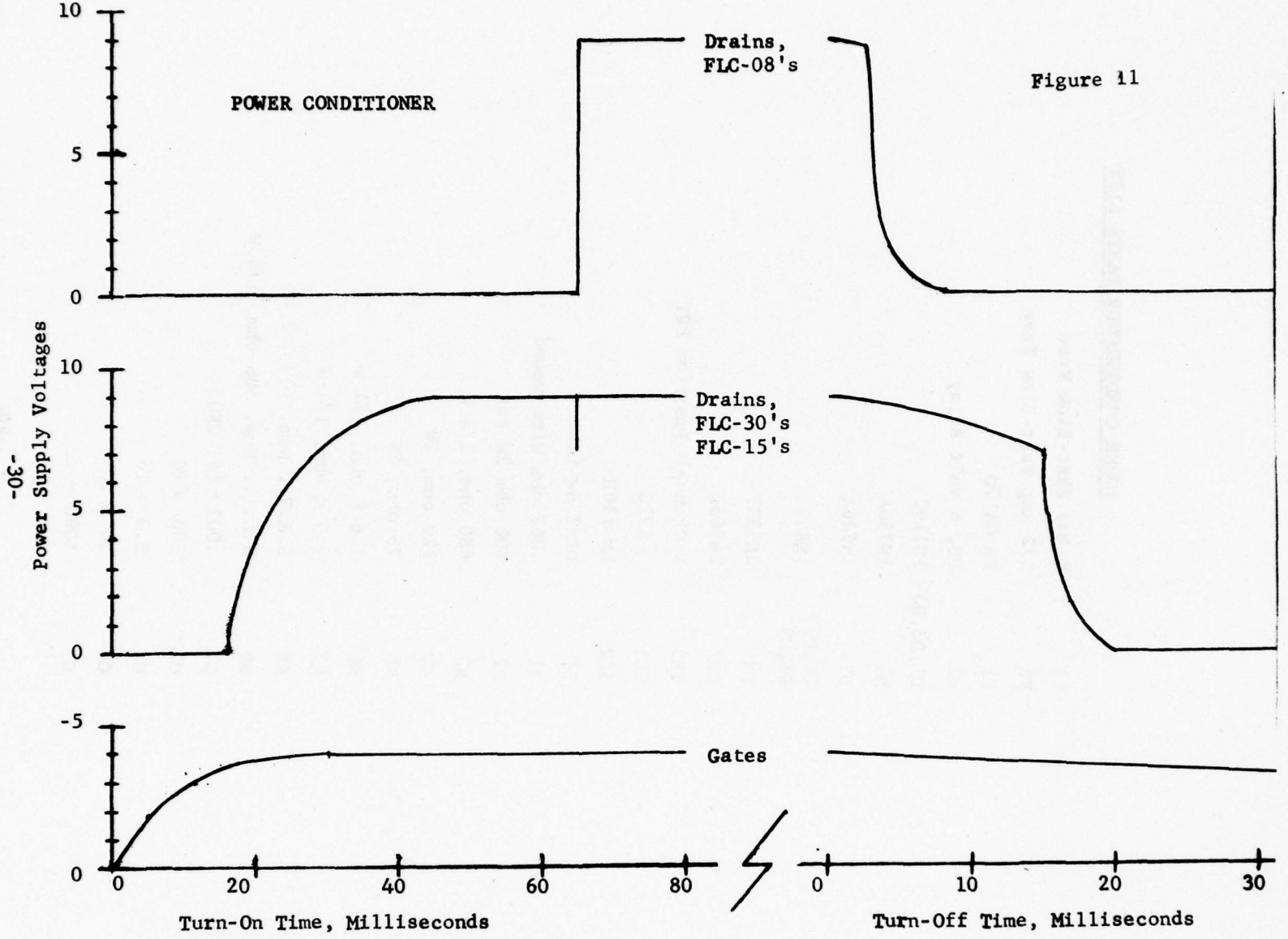

POWER CONDITIONER
Drains,
FLC-08's
10
5
0
Drains,
FLC-30's
FLC-15's
10
5
0
-30-
Power Supply Voltages
Gates
-5
0
0
20
40
60
80
Turn-On Time, Milliseconds
0
10
20
30
Turn-Off Time, Milliseconds

Figure 11

trated heat in the entire amplifier. Fans are provided on the end of the heat sink for cooling.

The picture in Figure 12 shows an isometric view of the entire amplifier with its top cover removed.

The picture in Figure 13 shows the front panel view of the amplifier.

The picture in Figure 14 is a straight down view of the completed microwave circuitry of the amplifier.

2.6 FINAL TEST RESULTS

The final test results will be divided into two parts. First, the final test data will be presented, evaluated and explained. Then, the Linear Solid State Communications Amplifier specifications will be compared to these results.

2.6.1 Test Data and Explanation

All of the test data presented here is for the entire power amplifier after final integration. It includes approximately .25 dB loss in the output circuit due to the isolator provided as an extra safety precaution to the user but does not include the .5 dB input cable loss.

The first set of curves are the RF power input vs RF power output transfer characteristics as shown in Figure 15. Nominal maximum input power for linear operation is 0 dBm. Maximum linear power output is 34.8 dBm or 3 watts. Maximum saturated power output is +38.1 dBm or 6.45 watts. Note that in the saturated mode, the 1 dB gain compression point is approximately .4 dB below maximum power output. This is primarily due to the cascading of many devices. The widening between the two curves toward saturation is due to peak power limiting.

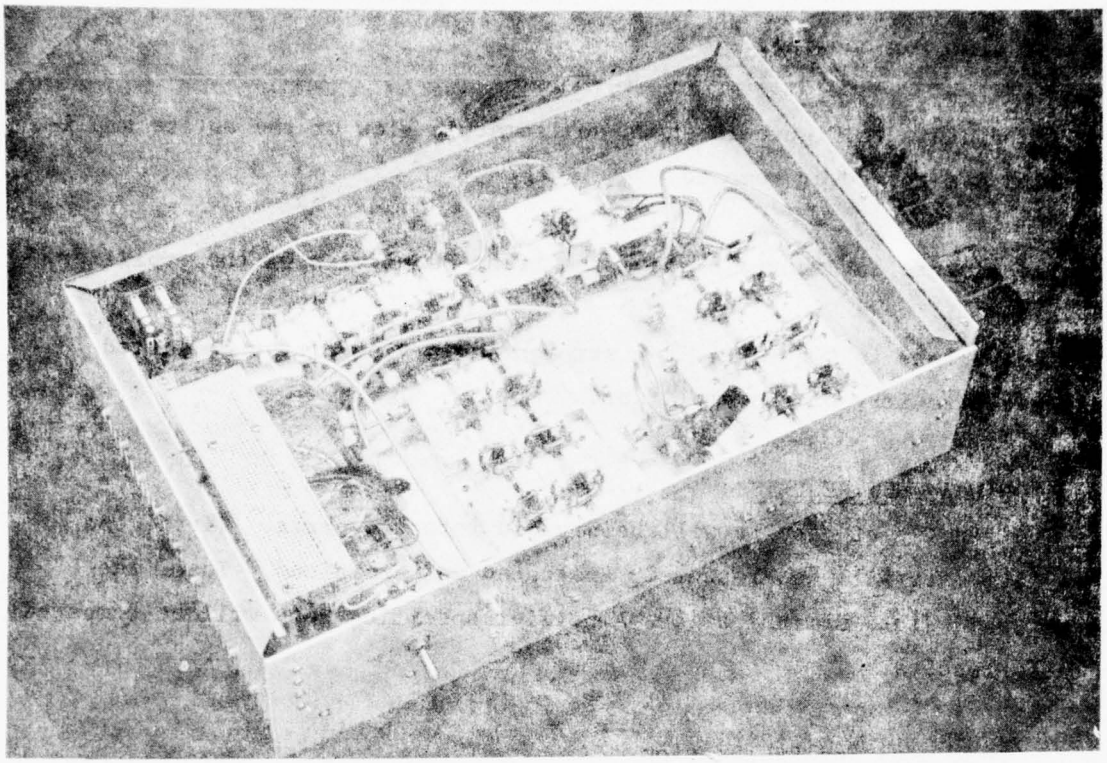


Figure 12

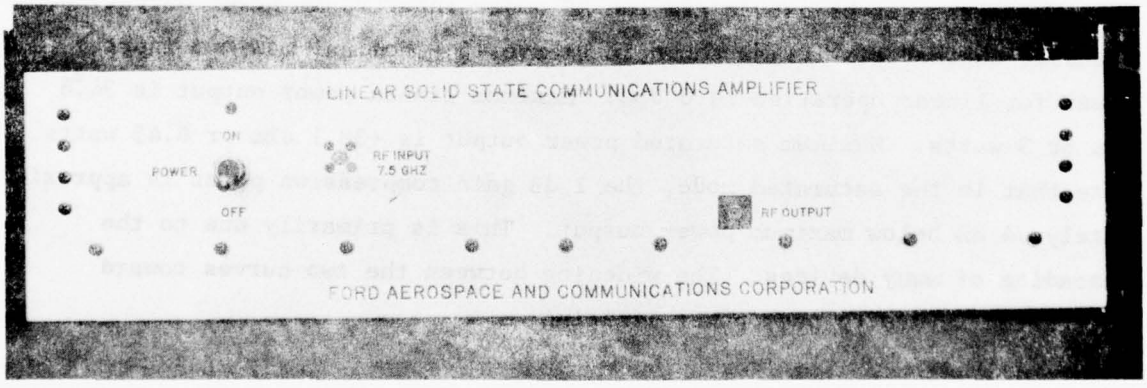


Figure 13

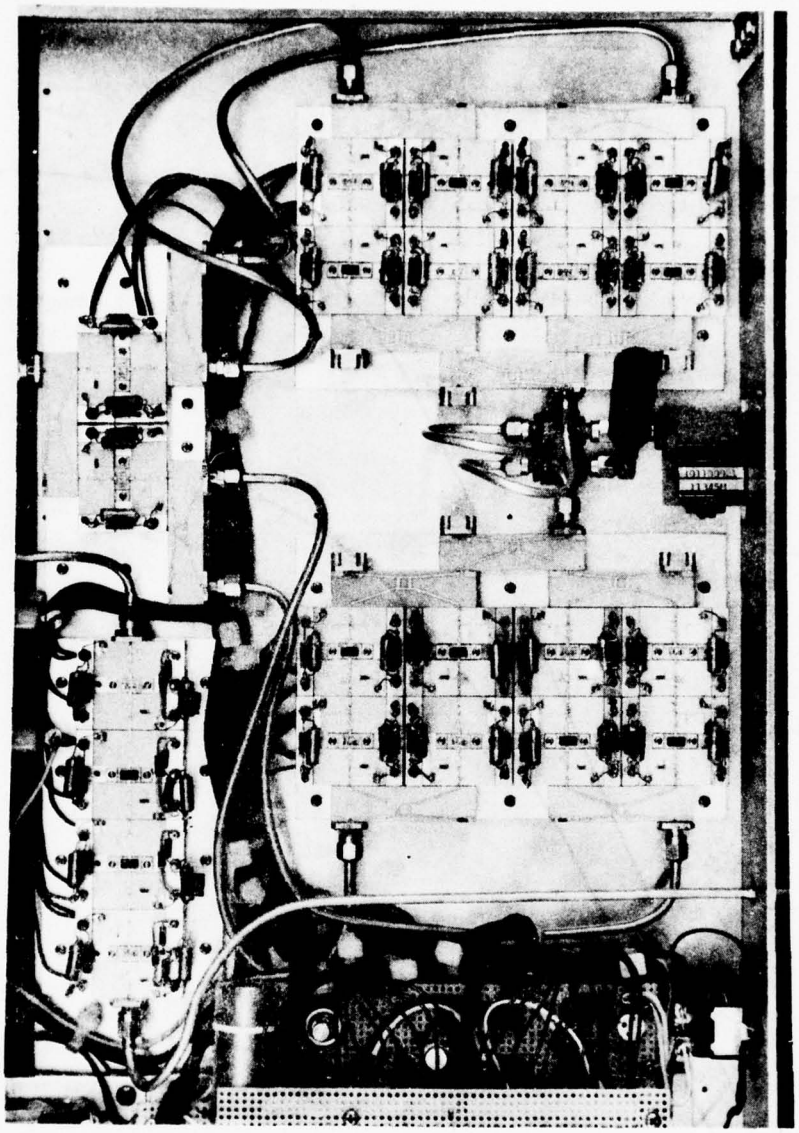
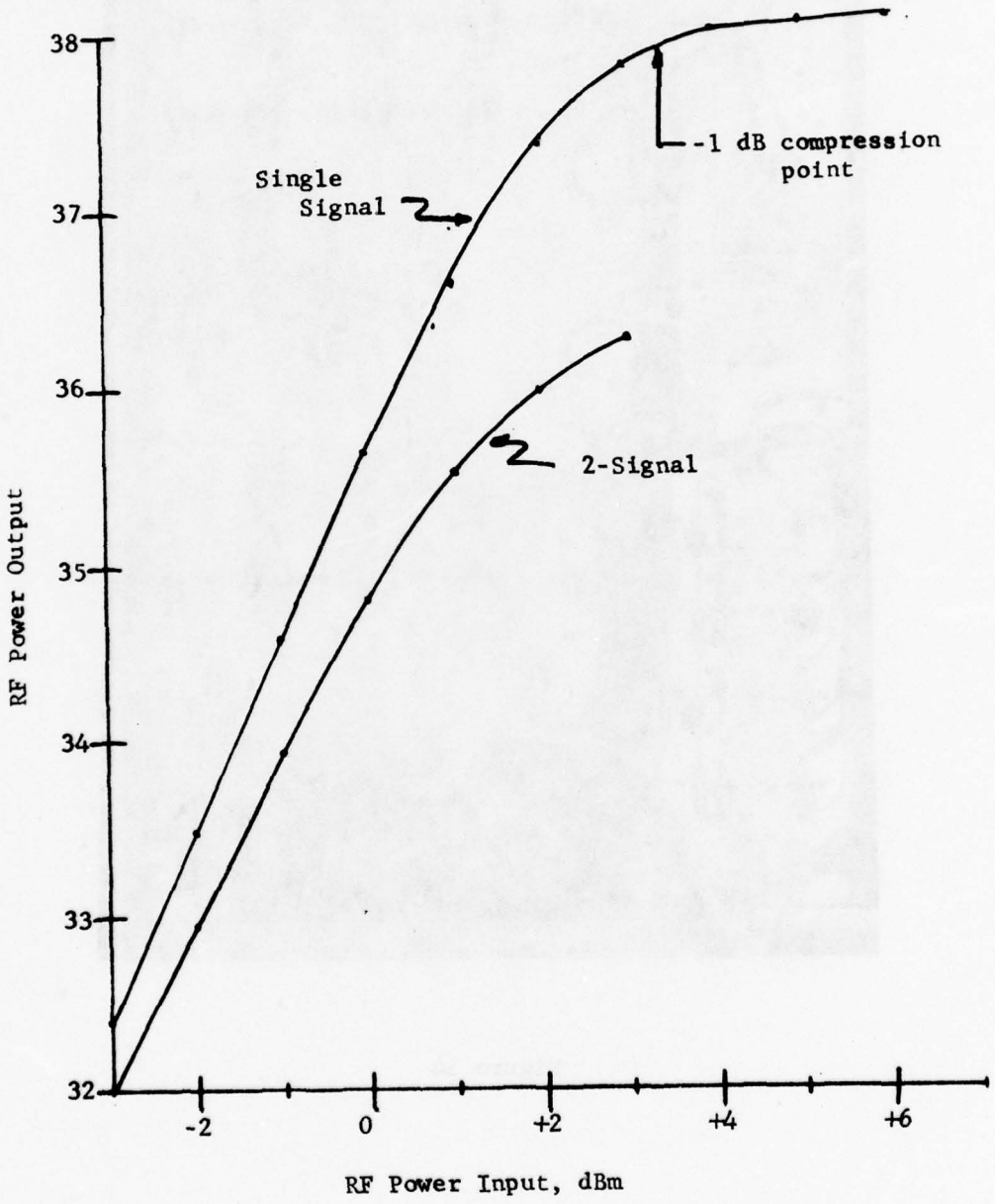


Figure 14

Figure 15

POWER TRANSFER CURVE

Frequency = 7.5 GHz



The next curve, Figure 16, displays intermodulation distortion vs RF power output for 2 signals. The IMD is third order products shown in dB below both of the two equal signals. The IMD in this linear amplifier is independent of the separation between f_1 and f_2 as long as both remain in the -1 dB bandwidth. The intermodulation distortion at the design frequency, 7500 MHz, is -30 dBc at the 3 watt power output level. At both upper and lower -1 dB band edge points, the IMD remains at -30 dBc.

The plateau that occurs at -31 dB IMD is a result of tuning and optimizing the amplifier for linear operation at given power levels.

Figure 17 is a graphical display of RF power output vs frequency for two signal operation. The -1 dB bandwidth is 160 MHz. The rise in power output at 7440 MHz was a complete surprise and resulted during final integration. The lower frequency limit is 7400 MHz and the upper frequency limit is 7560 MHz for linear operation at nominal power input of 0 dBm. The gain flatness is $\pm$ .25 dB/14 MHz as required in the specification.

The single signal RF power output vs frequency curves are shown in Figure 18. The power output scale on this graph is expanded compared to the previous figure. It is interesting to note that the 160 MHz bandwidth points are down approximately .5 dB. The -1 dB bandwidth was measured to be 210 MHz.

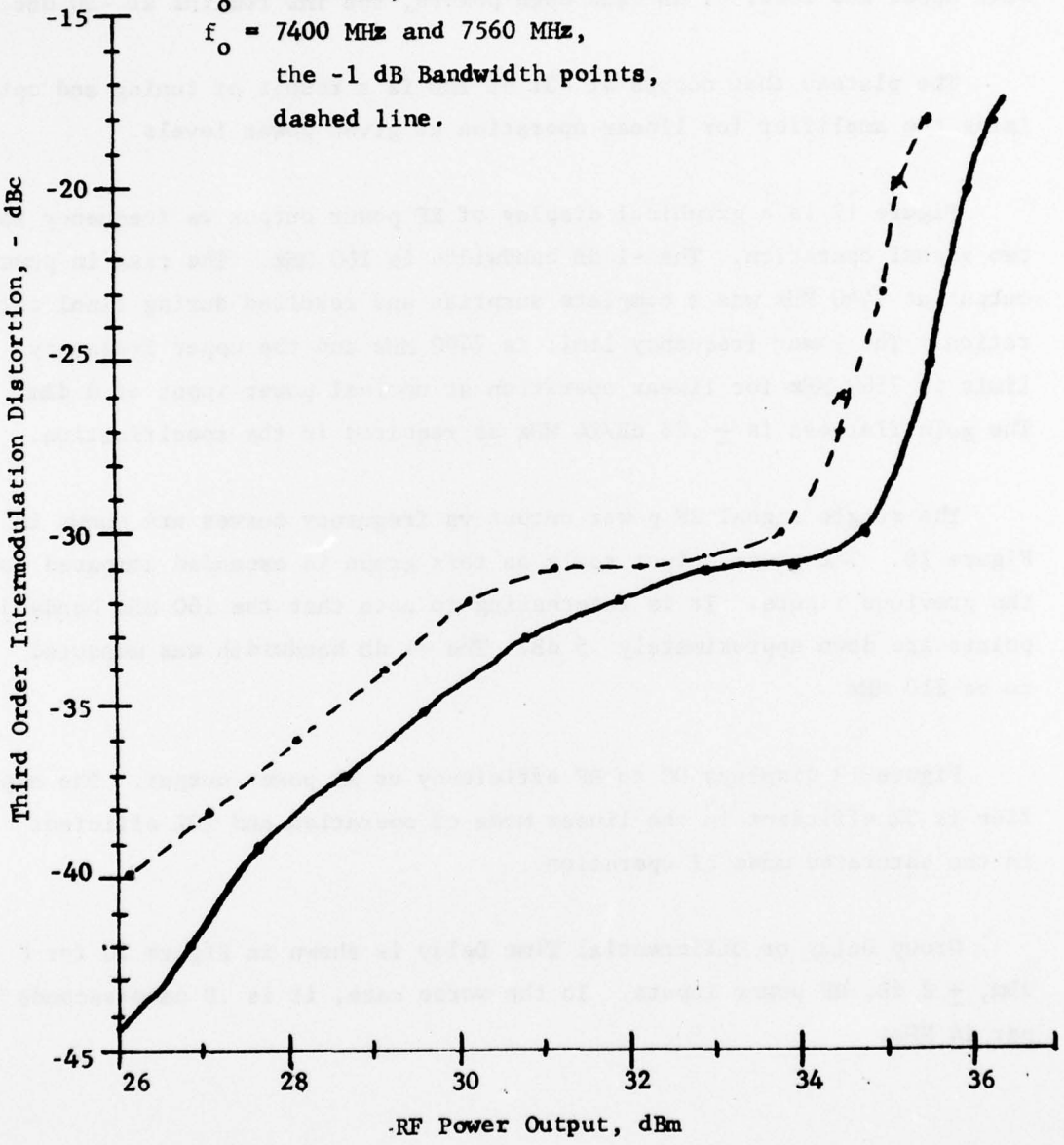
Figure 19 displays DC to RF efficiency vs RF power output. The amplifier is 5% efficient in the linear mode of operation and 10% efficient in the saturated mode of operation.

Group Delay or Differential Time Delay is shown in Figure 20 for 0 dBm, $\pm$ 2 dB, RF power inputs. In the worse case, it is .8 nano-seconds per 14 MHz.

Figure 16

IMD vs RF POWER OUTPUT, TWO SIGNAL

$f_1 - f_2$ = 10 MHz
f_o = 7500 MHz, Solid Line
f_o = 7400 MHz and 7560 MHz,
the -1 dB Bandwidth points,
dashed line.

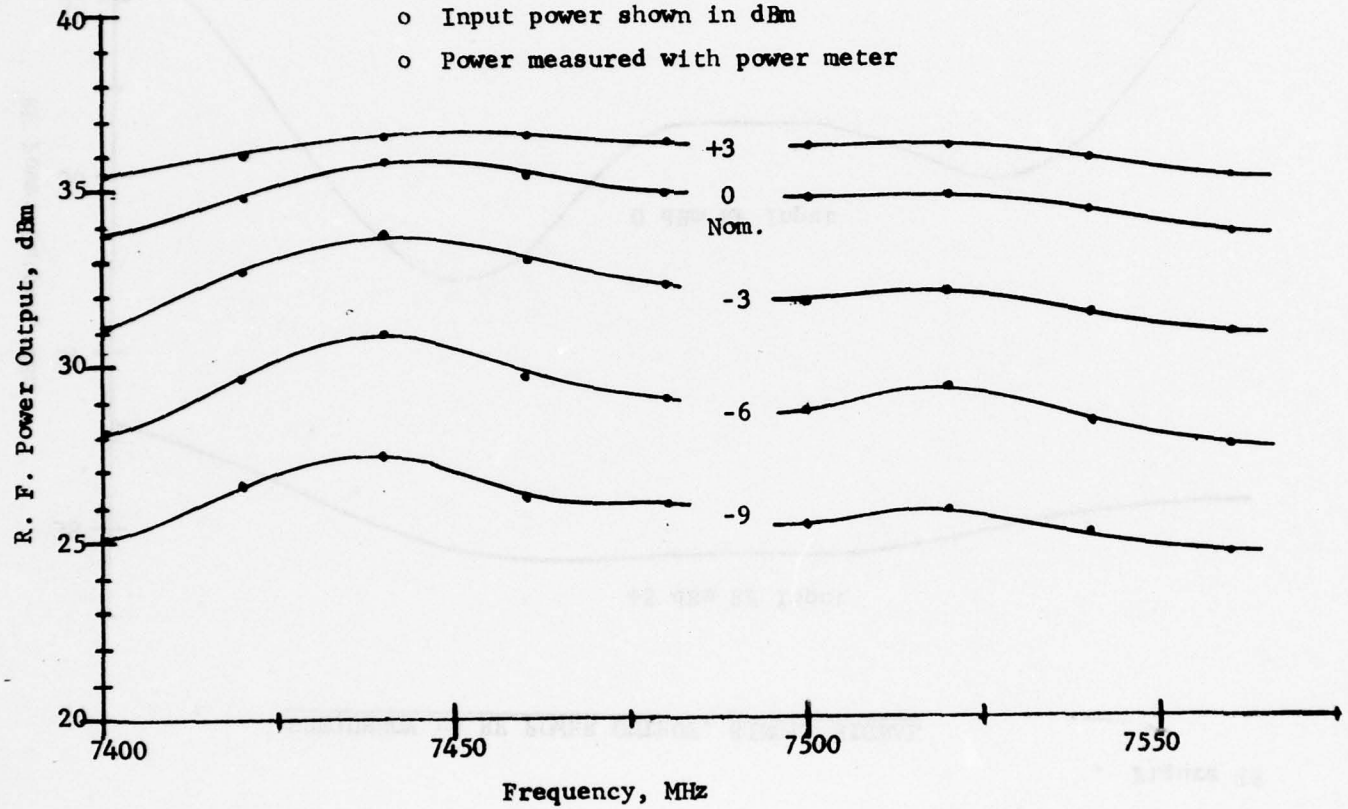


FREQUENCY vs RF POWER OUTPUT, TWO SIGNAL

Figure 17

Test Conditions:

- o 2 Signals, $f_1 - f_2$ = 10 MHz
- o Input power shown in dBm
- o Power measured with power meter



. Figure 18

FREQUENCY vs RF POWER OUTPUT, SINGLE SIGNAL

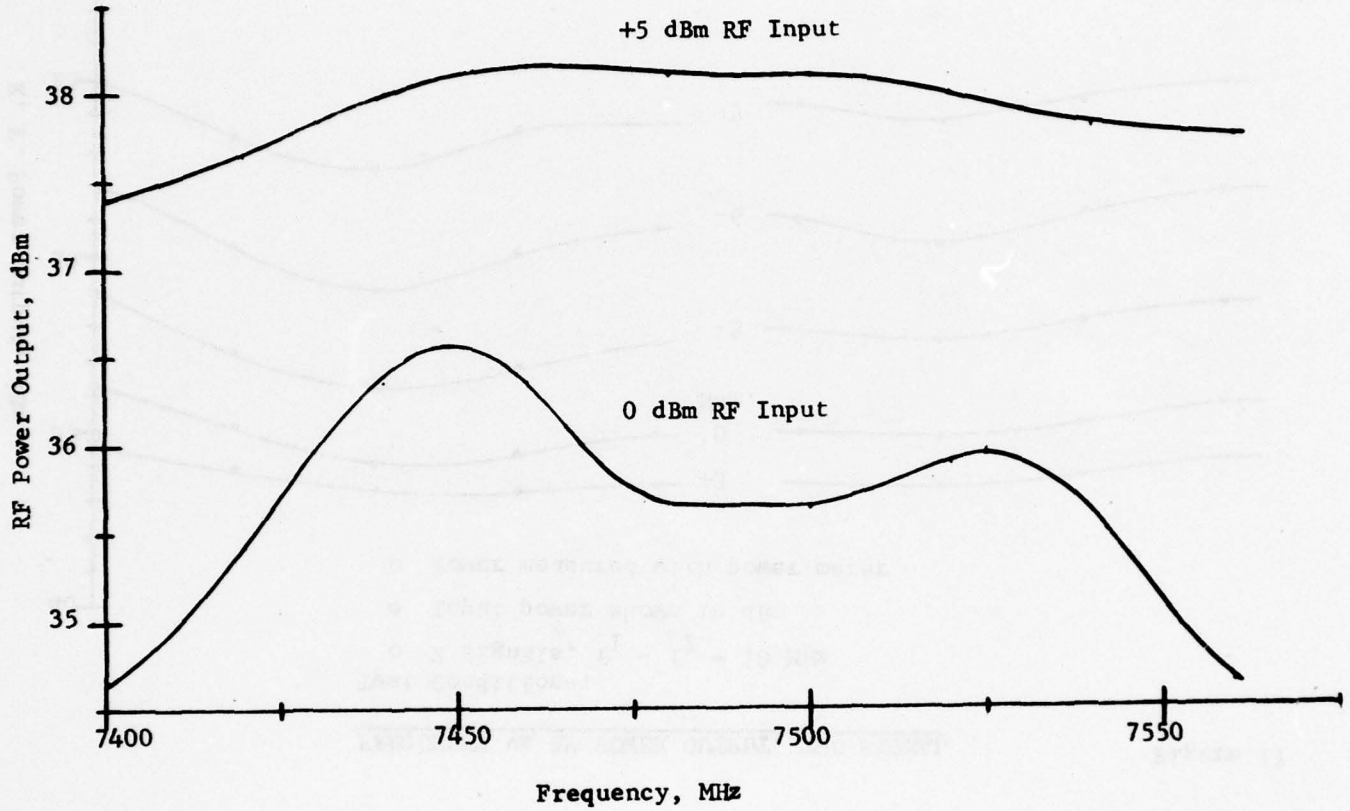


Figure 19

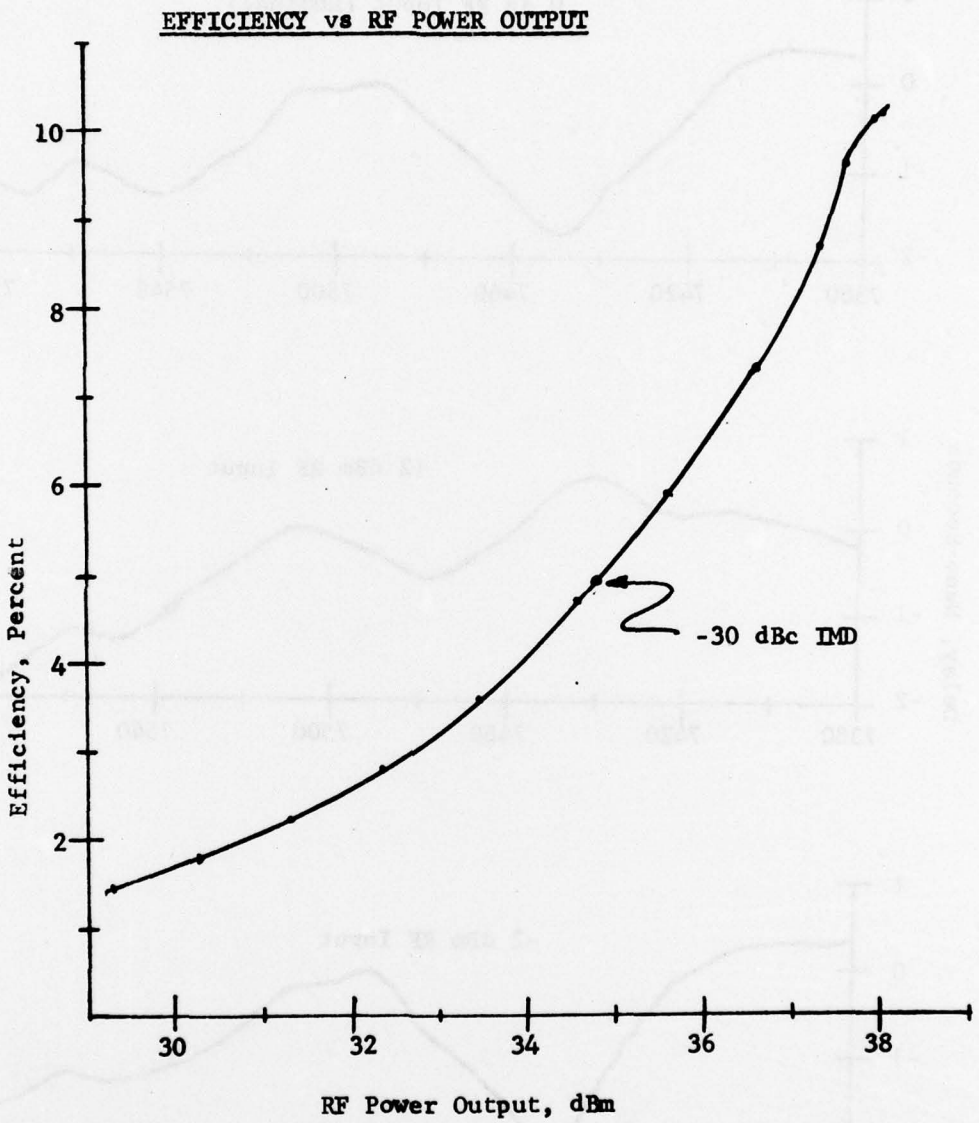
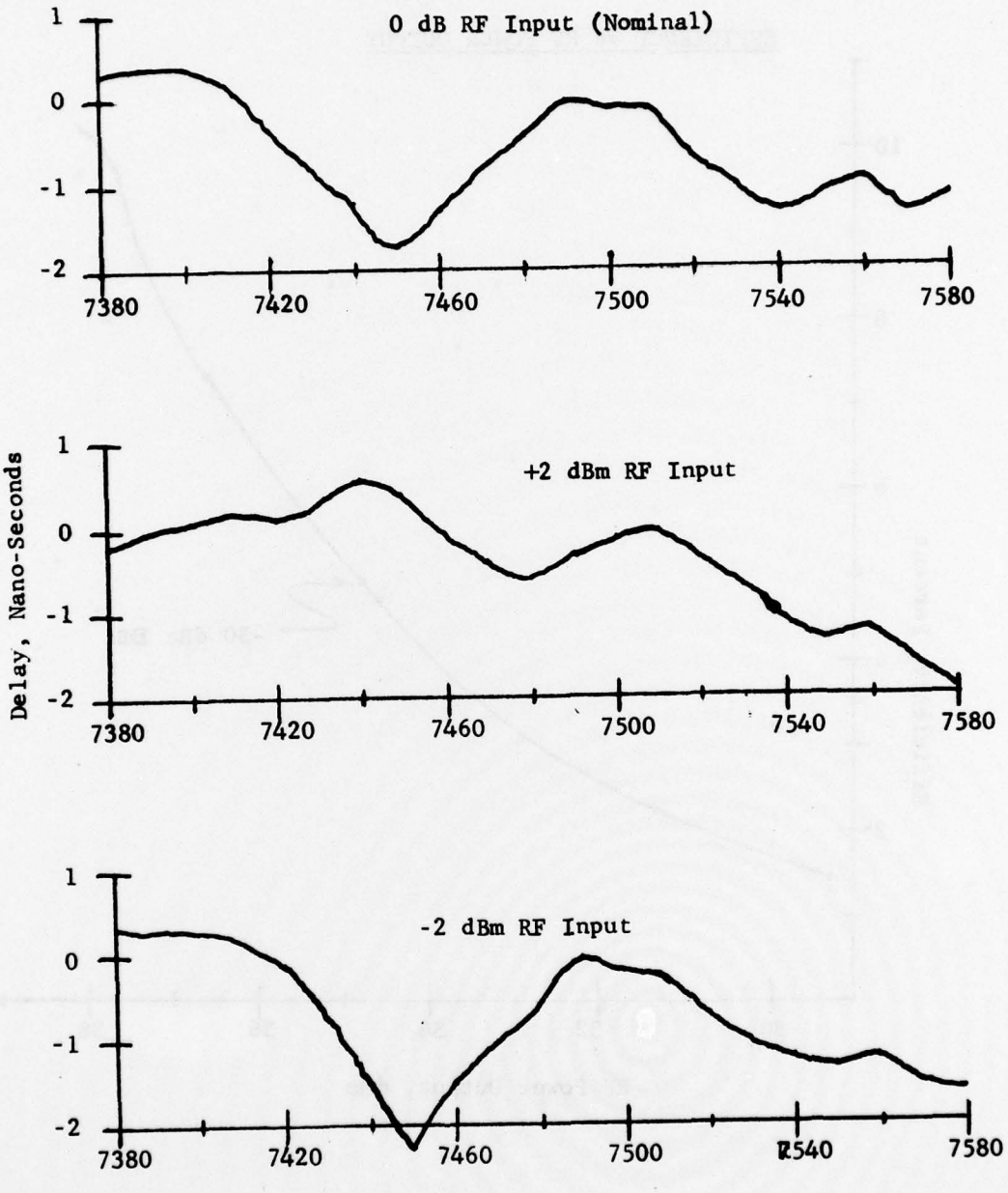

EFFICIENCY vs RF POWER OUTPUT
10
8
6
4
2
Efficiency, Percent
-30 dBc IMD
30
32
34
36
38
RF Power Output, dBm

Figure 20

GROUP DELAY



A true AM to PM conversion test was not possible to make. Therefore, relative phase vs RF input power changes were measured with a network analyzer. The resolution of this method, especially with all of the stray RF fields affecting the analyzer, is not as good as the .1 degree per dB specification. Figures 21 and 22 are a result of the test data taken. Their absolute validity are in question. They do indicate a .5 dB per degree maximum over the linear range of the amplifier. This is not consistent with the excellent linear IMD characteristics of the amplifier.

Across the 160 MHz -1 dB bandwidth of the amplifier, the VSWR measured less than 1.25:1 and the noise figure was a constant 8.7 dB. It should be noted that the input FET is not a low noise device, but a power FLC-08.

2.6.2 Specifications vs Results

The table below lists the performance of the Linear Solid State Communications Amplifier compared to the specifications.

Parameter	Specification	Performance
RF Power Output, Linear	1 Watt min. 5 Watts goal	3 Watts
RF Power Output, Saturated	None	6.5 Watts
Bandwidth	400 MHz @ 3 dB	160 MHz @ -1 dB, 310 MHz @ 3 dB
Gain	30 dB $\pm$ .25 dB/ 14 MHz	35 dB $\pm$ .25 dB/ 14 MHz
Noise Figure	30 dB Max.	8.7 dB
Third Order IMD	$\leq$ 30 dBc	-30 dBc
Spurious Signals	$\leq$ 80 dBc	$\leq$ 80 dBc
DC to RF efficiency (Linear)	10% min.	5%
DC to RF efficiency (Saturated)	None	10%
Differential Delay	1 ns/14 MHz max.	.8 ns/14 MHz
VSWR	1.5:1 max	1.25:1
AM to PM Conversion	$.1^{\circ}$/dB max.	$.5^{\circ}$/dB or less

Figure 21

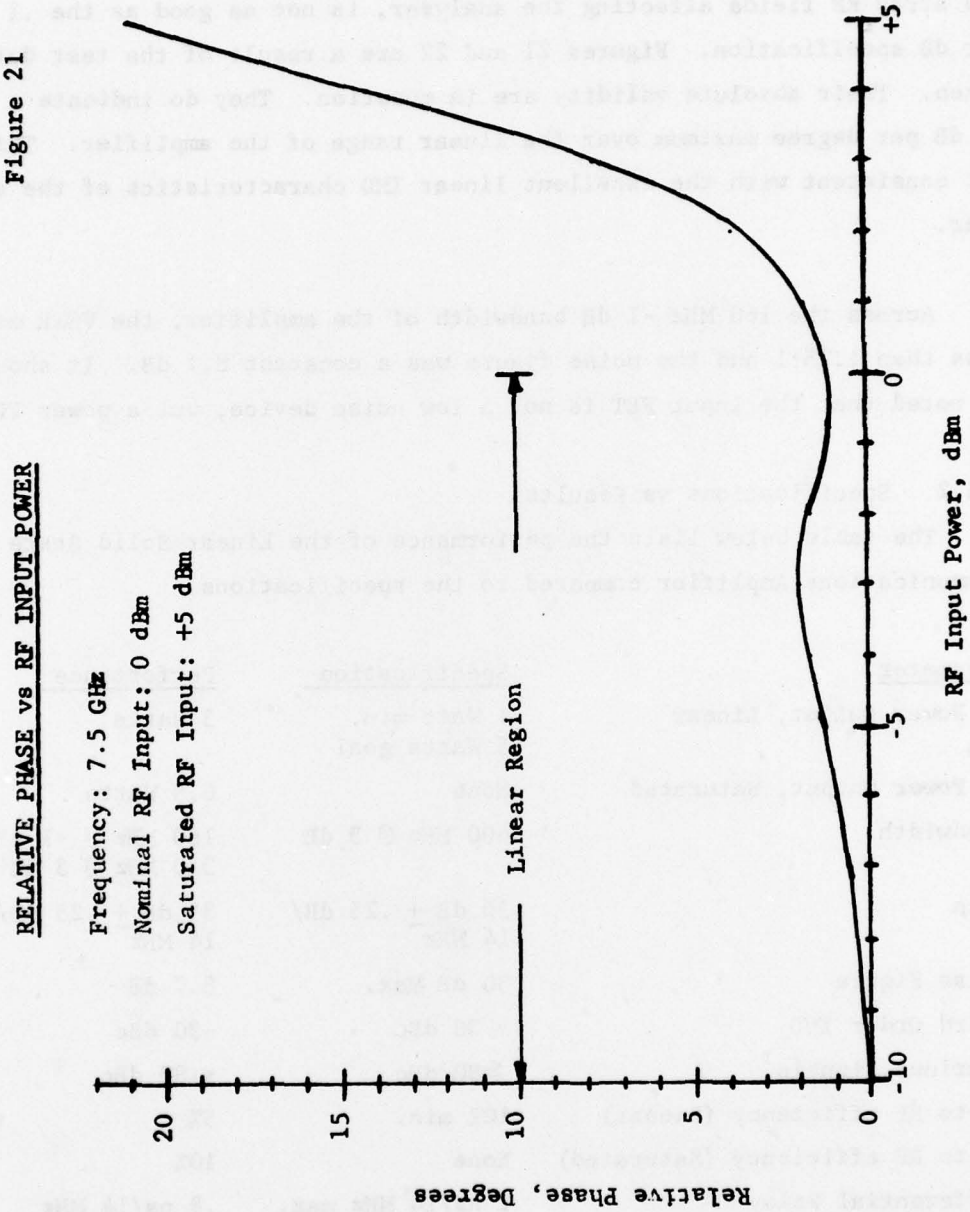
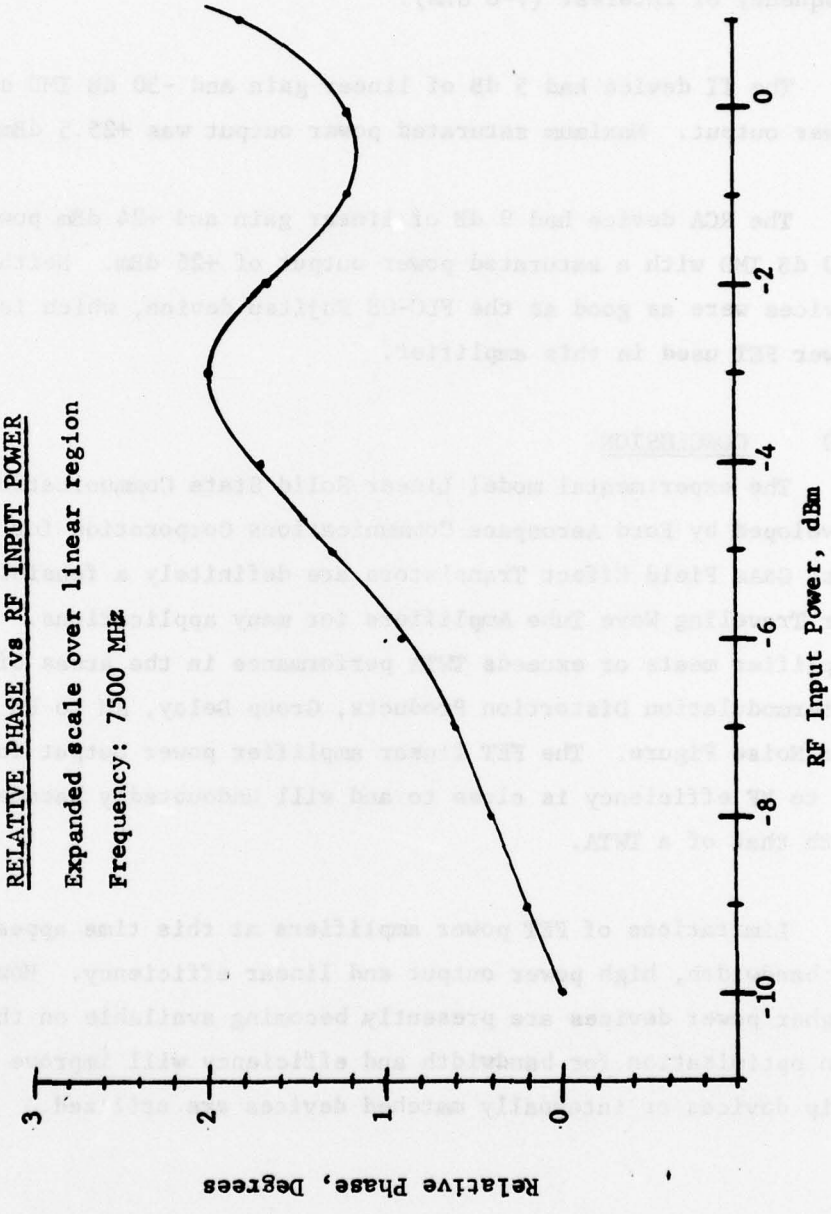

RELATIVE PHASE vs RF INPUT POWER
Frequency: 7.5 GHz
Nominal RF Input: 0 dBm
Saturated RF Input: +5 dBm
Linear Region
Relative Phase, Degrees
20
15
10
5
0
-10
-5
0
+5
RF Input Power, dBm

Figure 22


RELATIVE PHASE vs RF INPUT POWER
Expanded scale over linear region
Frequency: 7500 MHz
Relative Phase, Degrees
3
2
1
0
-10
-8
-6
-4
-2
0
RF Input Power, dBm

2.7 OTHER DEVICES TESTED

High power GaAs FET's developed by RCA and TI were evaluated on this program also. The devices were characterized using the Automatic Network Analyzer. Then test circuits were built to obtain useful data at the frequency of interest (7-8 GHz).

The TI device had 5 dB of linear gain and -30 dB IMD at +23.5 dBm power output. Maximum saturated power output was +25.5 dBm.

The RCA device had 9 dB of linear gain and +24 dBm power output at -30 dB IMD with a saturated power output of +26 dBm. Neither of these devices were as good as the FLC-08 Fujitsu device, which is the lower power FET used in this amplifier.

3.0 CONCLUSION

The experimental model Linear Solid State Communications Amplifier developed by Ford Aerospace Communications Corporation for RADC has proven that GaAs Field Effect Transistors are definitely a feasible replacement for Traveling Wave Tube Amplifiers for many applications. The FET linear amplifier meets or exceeds TWTA performance in the areas of linearity, Intermodulation Distortion Products, Group Delay, AM to PM conversion, and Noise Figure. The FET linear amplifier power output for an associated DC to RF efficiency is close to and will undoubtedly become competitive with that of a TWTA.

Limitations of FET power amplifiers at this time appear in the areas of bandwidth, high power output and linear efficiency. However, much higher power devices are presently becoming available on the market. Design optimization for bandwidth and efficiency will improve when unpackaged chip devices or internally matched devices are utilized.

This development effort proved the feasibility of power combining many parallel devices. It also demonstrated a need for minimizing output power combining losses when doing so. Techniques, skills, and capabilities to use high power FET's and avoid destruction of the devices were developed and proven.

All of the exact specifications were not quite met. However, the results were sufficient to prove that GaAs FET amplifier will be the solid state amplifiers of the future. At this time, Fujitsu and other device makers are gathering excellent reliability data that should prove that GaAs FET amplifiers are more reliable and have a higher mean time to failure than TWTA's.

4.0 RECOMMENDATIONS

Further development work is necessary and should be approached in the areas of bandwidth, efficiency, and higher power output. It would also seem reasonable to improve IMD performance with future work. The following list of recommendations will provide improved performance necessary for future amplifier requirements:

- Improved circuit optimization using computer aided design networks.
- Sophisticated mechanical design.
- Use of chip devices.
- Use of higher power output devices or more multiple stages.
- Minimizing the output losses due to mechanical layout and power combiner design.
- Elimination of directly cascaded stages in the high power portions.

5.0 APPENDIX

LINEAR SOLID STATE COMMUNICATIONS AMPLIFIER

OPERATING INSTRUCTIONS

The following operating instructions and precautions are presented here in order to prevent operational damage to the Linear Solid State Communications Amplifier. Although Solid State FET amplifiers offer increased life time and reliability over TWTA's, they are unforgiving to associated equipment failure and to human errors. A power supply conditioning circuit is built into the amplifier to regulate supply voltages, assure proper sequential turn on and off of the FET amplifiers, and to prevent failures due to untimely power line outages. The instructions listed below are necessary good engineering practices to prevent damage due to human or associated equipment failures.

1. Two D. C. power supplies are required. One for +16 volts (nom.) at 8 amps (min.) and the other for -10 volts (nom.) at 1/2 amp (min.).
2. Always turn on power supplies BEFORE turning amplifier switch "ON".
3. Check out both power supplies for any oscillations from no load up to full rated loads. This should include their turn-on and turn-off oscillations in case of A. C. line intermittant failure. No oscillations should be present.
4. Upon initial turn-on of amplifier, reset power supplies for correct voltages at the back panel of the amplifier. Reset voltage of -10 volt supply first.
5. Never turn-on amplifier with RF input signal applied. (This is only a safety measure and is not necessarily mandatory.)

6. Maximum power input for linear operation is 0.5 dBm. Absolute maximum RF power input is +6 dBm. (Due to the linear optimization techniques designed into the amplifier, no input limiter is provided.) The above mentioned linear power level limits are for RMS RF power as measured by a power meter of continuous multi-tone and single tone signals.
7. Nominal RF output levels are 3.1 watts linear (-30 dB IMD, 2-tone) and 6.4 Watts saturated single signal or narrow band F.M.
8. Design center frequency is 7500 MHz.
9. The amplifier will not achieve full operational specifications until turned on for five minutes. This is due to power conditioner warm-up to supply the correct voltages. The FET amplifier is not temperature sensitive.
10. A fan is supplied to blow air across the heat sink fins located on the bottom. Please use this or an equivalent fan at all times that the amplifier is "ON".
11. A plexiglass top is provided to allow viewing of the MIC circuitry without endangering the tuned circuitry to curious probing.
12. Power supply leads of #18 Ga wire or larger should be used. Space lugs should be used at the rear power input terminal of the amplifier. Separate common return wires MUST be used for each of the two power supplies.
13. An output isolator is provided in the amplifier. However, as always, good engineering practice is to always load the output with a reasonably good R. F. load at the operating frequencies.

LIST OF ABBREVIATIONS AND SYMBOLS

FET	Field Effect Transistor
GaAs	Gallium Arsenide
IMD	Intermodulation Distortion
VSWR	Voltage Standing Wave Ratio
D.C.	Direct Current
TWTA	Traveling Wave Tube Amplifier
MHz	Megahertz
GHz	Gigahertz
Vp	Peak Voltage
Vm	Minimum Voltage
Pav	Average Power
PEP	Peak Effective Power
MEP	Minimum Envelope Power
P/A	Peak to Average Ratio
RF	Radio Frequency
η	Efficiency
SAT	Saturated
Δ	Delta, Change
ω	Omega, 2π times frequency
t	time
Idc	Direct current
dB	Decibel
dBc	dB reference to carrier

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Printed by
United States Air Force
Hanscom AFB, Mass. 01731